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Defect-less Monolithic Low-k/Cu Interconnects by Chemistry-controlled CMP

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1. Introduction

In order to realize high performance and low power dissipation in scaled down LSIs, a full low-k interconnect structure without SiO_2 (k~4.5) hard masks (HM) is inevitably needed. The key process for SiO_2 HM less structure is CMP and post-CMP cleaning, since a low-k film with hydrophobic surface and low modulus is exposed (Fig.1). The low modulus causes scratch and delamination during the over polishing, requiring precise end-point detection (EPD) system. The hydrophobic surface makes the post-CMP cleaning difficult. In this work, we investigated the effect of CMP process on the low-k monolithic structures using a local-CMP technology [1-4].

2. Experimental

Fig.2 describes the features of a local CMP, where the CMP pad with smaller diameter than 300mm-wafer scans a face-up wafer on the rotating chuck. This actualizes precise in-situ optical EPD based on the reflection spectra from the polishing surface. When the Cu film is thinner than 100nm, the reflection intensity starts to decrease because of the transparency. As the result, we can detect the Cu thickness of 100nm as T_0 in the on-current CMP. After the Cu is removed completely, the Cu clear is detected as T_1. The over-polishing time (OPT) is set for the time difference such as $\alpha(T_1-T_0)$. Namely, regardless of the initial Cu thickness, the EPD method estimates the "on-current" Cu CMP rate of the last 100nm-thickness, enables us to set precise OPT with "wafer by wafer". An example of the EPD system is shown in Fig.3. The precise EPD is a key to reduce CMP defects during OPT especially for low-k monolithic structure.

3. Results and discussion

3-1: Basic low-k CMP properties

We investigated basic CMP properties for several low-k films (Table 1). Each blanket film was polished for 50sec under the pressure of 2.0psi. After CMP, defects were detected by a defect inspection system and classified.

By CMP with SiO_2 slurry containing oxidizer chemicals, the C/Si ratio of the low-k surface was decreased, while the O/Si ratio was increased (Fig.4). The hydrophobic low-k surface without the CMP exhibited large contact angle to a de-ionized water (DIW) droplet, resulting in high defect density (Fig.5). Most of the defects were found to be organic residues and watermarks. The samples with the CMP, however, had small contact angle and less defect density than the sample without CMP. The CMP made the low-k surface hydrophilic by the surface oxidation reacted with the slurry, achieving defect density as small as SiO_2.

3-2: Surface cleaning on low-k film after CMP

In actual CMP process with Cu patterns, we have to care Cu organic complex residues during the post-CMP cleaning. In order to suppress Cu complex residues, we need to control the oxidation-reduction potential (ORP) of the cleaning chemicals [5]. Fig.6(a) compares Cu intensity on the SiOCH (k=3.1) area in a patterned wafer after CMP, detected by TOF-SIMS analysis. Compared with DIW rinse after brush scribe, the alkalized water rinse with ORP~-0.7V decreased the Cu concentration remained on the SiOCH film, resulting in tighter distribution of the breakdown electric field (E_{bd}) between adjacent lines (Fig.6(b)). These results indicate that the control of the ORP of the cleaning chemical is of great importance to suppress Cu organic residues and obtain superior dielectric properties in the low-k monolithic structure (Fig.7).

3-3: Interconnect performances

The low-k monolithic structure had less increase in the line resistance during barrier metal (BM) CMP time than the SiO_2 monolithic structure (Fig.8). This is because the polishing rate of the low-k film was 1/10 smaller than that of SiO_2 film. The CMP self-stop nature of the low-k structure as well as the precise EPD system suppressed deviation in the interconnect parameters against CMP over polishing. Fig.9 plots the C-R of the L/S=100/100nm lines. The inter-line capacitance in the low-k structure was reduced by 20% than that in the SiO_2 one, while the dispersion in C-R was smaller in the low-k than in the SiO_2. The worst-case C-R characteristic was improved by 31%. Fig.10 shows the distribution of the E_{bd} measured by comb-wiring pattern with L/S =90/90nm and the 80mm parallel length. Optimizing ORP of cleaning chemicals, the low-k structure found to show comparable E_{bd} distribution to the SiO_2 one.

4. Conclusions

Defect-less monolithic low-k/Cu interconnects have been obtained for low parasitic capacitance LSIs. The change in low-k surface from hydrophobic to hydrophilic by the CMP slurry with oxidizer, and the control of ORP of cleaning chemical are essential for achieving superior dielectric property in the low-k monolithic structure. The defect-less low-k_{eff} Cu interconnect is practical for digital-consumer and automotive applications.

Acknowledgements

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References

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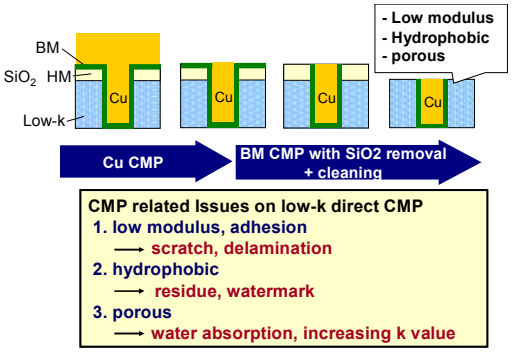

Fig.1 CMP related issues on low-k direct CMP.

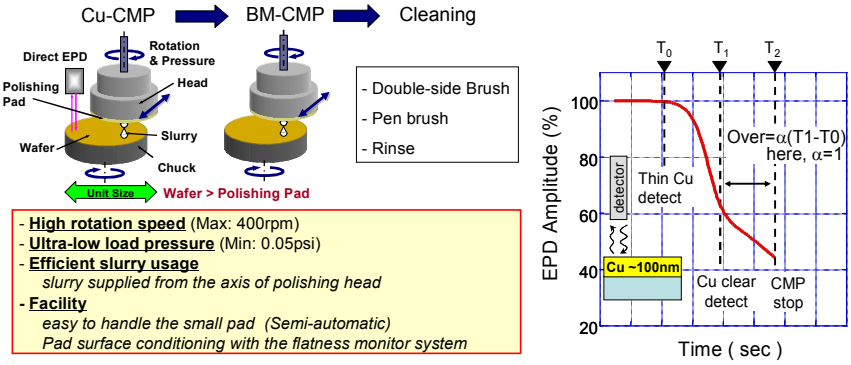

Fig.2 The CMP tool used for this experiment with a flexible thin-Cu end point detection (EPD) method using white-light interferometry, in which the under-layer can be detected through the Cu film less than 100nm-thick.

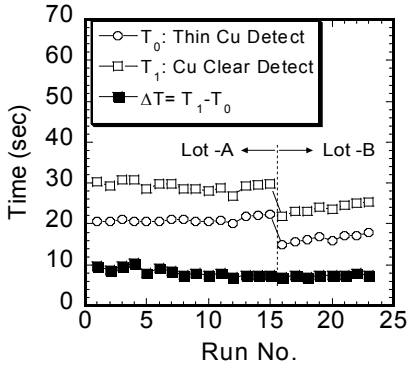

Fig.3 The EPD time for Cu CMP with the different Cu initial thickness (Lot-A > Lot-B). ΔT: T_1-T_0, didn't change between the Lots, indicating the Cu removal rate was identical.

Table 1 Film properties

	SiO_2	SiOCH -A	SiOCH -B	SiOCH -C	SiOCH -D
k-value	4.5	3.1	3.1	2.7	2.5
Modulus (GPa)	80	13	20	6.5	3.0
Density (g/cm3)	2.3	1.5	1.4	1.3	1.1
C/Si ratio	0	0.6	1.1	0.6	2.7
Contact angle(°)	30	86	77	60	95

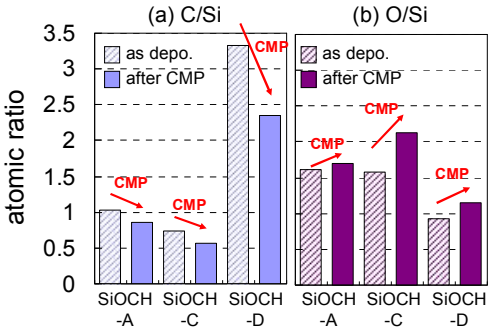

Fig.4 Surface chemical composition; (a) C/Si and (b) O/Si atomic ratio measured by XPS analysis.

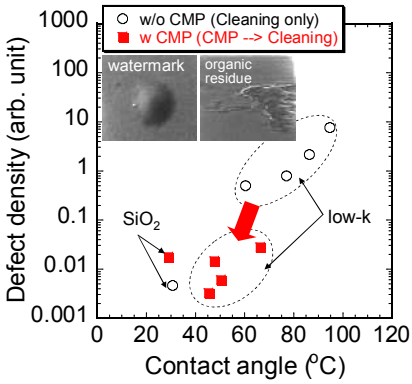

Fig.5 Defect density vs. contact angle between SiOCH surface and DIW droplet.

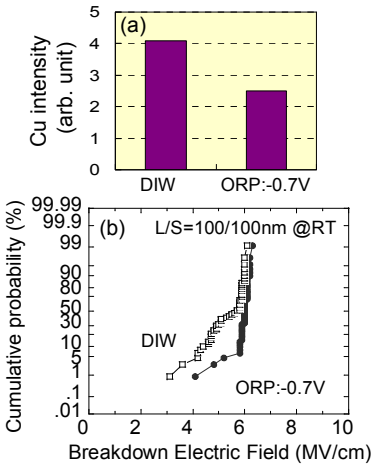

Fig.6 Effect of post-CMP cleaning on (a) SiOCH surface Cu concentration and (b) the breakdown electrical field (E_{bd}) in the 200nm-pitched lines.

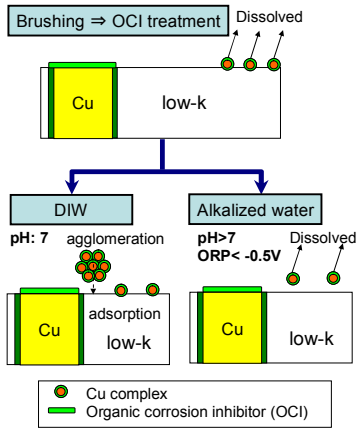

Fig.7 Post-CMP cleaning mechanism rinsed with DIW and Alkalized water.

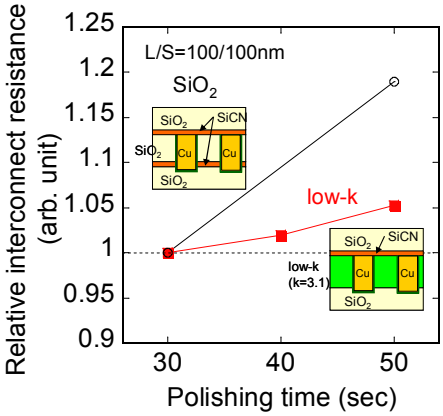

Fig.8 ρ_s change as a function of the barrier metal (BM) CMP time.

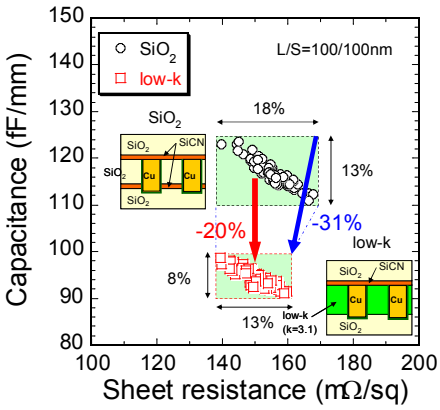

Fig.9 C-R plots for the L/S=100/100nm interconnects.

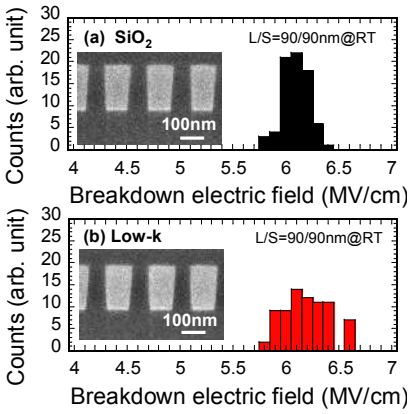

Fig.10 Distribution of the breakdown electric field (E_{bd}). (a) SiO_2, (b) low-k