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# Low Temperature Processes using Ni-induced Crystallization Technique for Monolithic Three Dimensional Integration

Jin-Hong Park[1], Munehiro Tada[1,2], Hailin Peng[3], and Krishna C. Saraswat[1,3]
[1] Department of Electrical Engineering, Stanford University, Stanford, CA 94305, USA
Phone: +1-650-862-6782 E-mail: jhpark9@stanford.edu
[2] Device Platforms Research Laboratories, NEC corporation, Sagamihara, Kanagawa, Japan
[3] Department of Materials Science Engineering, Stanford University, Stanford, California 94305, USA

## 1. Introduction

In this work, we have investigated very low temperature (1) single crystal Ge growth method by metal (Ni)-induced lateral crystallization (MILC) and (2) boron activation technique in α-Ge using metal (Ni)-induced crystallization (MIC) for 3D integration of P-channel Ge MOSFETs (Fig. 1) [1]. Self-nucleation and Ni-MILC of α-Ge films on $SiO_2$ are investigated, first, in an unconfined plane α-Ge films. The found conditions are subsequently applied to a patterned nanowire to obtain a single-crystal Ge wire on an insulating substrate at 360ºC without the deleterious effects of thermally induced self-nucleation. Ni not only successfully crystallizes α-Ge, it also facilitates activation of the boron atoms in the α-Ge during the crystallization process at temperatures as low as 360ºC. The feasibility of the low temperature activation technique has successfully been demonstrated for a Ge gate electrode in a Si P-channel MOSFET using Schottky Ni silicide source/drain.

The methods are promising for integrating high quality Ge transistors at low temperatures as required by 3D ICs.

## 2. Experiment and Results

***Single Crystal Ge Growth using MILC at 360 ºC***

Because self-nucleation is a competing process resulting in small crystallites, it is important to find self-nucleation free temperature if bigger crystallites are desired. According to the XRD analysis in Fig. 2, self-nucleation begins around 400ºC. Above 450ºC, the Ge (111) peak intensity saturates implying that the crystal size does not increase. However, our TEM analysis in Fig. 3 suggests that the temperature at which self-nucleation commences is a bit lower around 380ºC. Based on these results, 360ºC was determined to be a safe, self-nucleation free, temperature for subsequent MILC and MIC experiments. The Ni MIC sample is, subsequently, annealed for 1 hour in the temperature range of 300-450ºC. XRD data in Fig. 2 shows that the 200nm thick α-Ge film is fully crystallized by Ni at or above 350ºC.

Next, we create a narrow single crystal Ge wire. The idea is to achieve this by having a grain size larger than the line dimensions, and to propagate a single grain laterally through a narrow α-Ge wire. First, we obtain a Ge line about 70nm wide and 100nm thick using resist trimming process (Fig.4). Subsequently, we anneal this Ge nanowire for 5 hours at 360ºC. We find ~1.33μm lateral growth yielding a growth rate of ~0.266μm/hr at 360ºC. Interface between poly-Ge and α-Ge is studied with both HRTEM and SAED patterns (Fig. 5). The wires are not completely single crystal because the grain size is found to be smaller than wire dimensions.

In a subsequent experiment, the α-Ge line thickness is reduced to 50nm (Fig. 6). As a result, fully single crystal Ge regions with roughly 120nm length are obtained. In this case, the MILC growth rate (~80nm/hr) is found to be lower than in the case of the 100nm α-Ge wire thickness (~0.266um/hr).

***Boron Activation in α-Ge using MIC at 360 ºC***

A 200nm thick α-Ge film is deposited at 300ºC by LPCVD onto a thermally grown 200nm $SiO_2$ on a Si (100) substrate. The α-Ge film is subsequently implanted by $BF_2$. A 5nm Ni film is deposited on α-Ge layer, and the sample is isothermally annealed in a $N_2$ ambient for 1 hour at 360ºC (Fig. 7). Since Ni has a high diffusivity in α-Ge, 1 hour at 360ºC is enough time to fully crystallize the 200nm α-Ge [2]. Poly-Ge is obtained after annealing for 1hour at 360ºC with Ni assistance, whereas, no change is observed in α-Ge film without Ni. Because boron atoms in the film are rearranged and activated during the crystallization process, an extremely low resistivity of 5.82mΩ·cm is obtained after annealing for 1 hour at 360ºC (Fig. 7). The amount of MIC activated boron in group #1 is only slightly lower than in group #2 activated by thermal annealing at 600ºC, since the resistivity of p-type Ge film in group #1 is only slightly higher than that of p-type Ge film in group #2. Comparing undoped Ge film of group #1 with undoped Ge film of group #2 and considering the XRD profiles (thermally annealed undoped Ge sample has higher XRD peaks than MIC undoped Ge sample), we find that Ni itself seems to contribute to only slight reduction in the resistivity of the film. The low temperature boron activation technique featuring the Ni-MIC is applied to form a gate electrode in Si PMOSFET combining with Schottky nickel silicide S/D at 360ºC. TEM image in Fig. 8 clearly shows the fully crystallized poly-Ge gate electrode, and C-V curve at 1MHz of the sample annealed at 360ºC is almost same as one of the sample annealed at 600ºC. The transistor (L=100um, Ring shape) operation such as $I_{SD}$-$V_{GS}$ and $I_{SD}$-$V_{DS}$ characteristics is also obtained in a fully low temperature process below 360ºC

## 3. Conclusions

We have demonstrated low temperature single crystal Ge growth and dopants (boron) activation in α-Ge on insulating substrate using MILC and MIC at 360ºC, respectively. These techniques are promising for integrating Ge transistors at low processing temperatures as required by 3D ICs.

**Acknowledgements**

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**References**

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[2] Ling Y. Wei, J. Phys. Chem. Solids, Vol. 18, pp. 162-174 (1961).

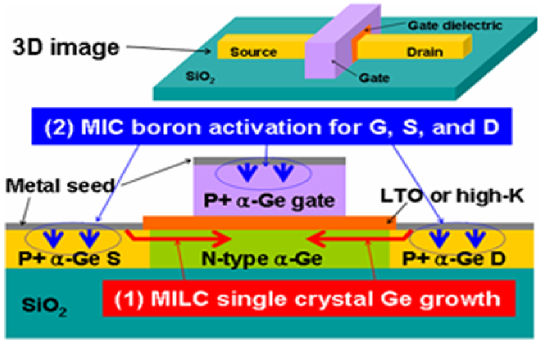


Fig. 1 Schematic image of P-channel Ge MOSFET on $SiO_2$ for 3D Integration.

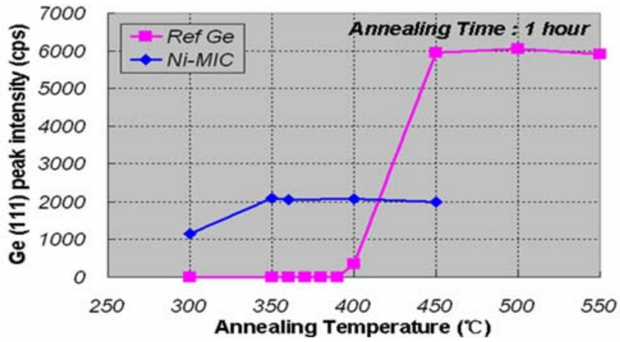


Fig. 2 Ge (111) intensity in XRD measurement as a function of post-annealing temperature of α-Ge

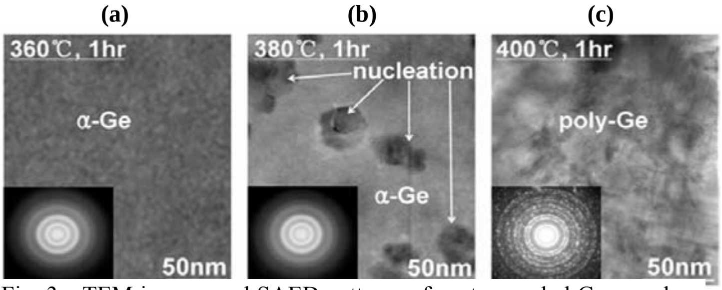


Fig. 3 TEM images and SAED patterns of post-annealed Ge samples at (a) 360°C, (b) 380°C, and (c) 400°C.

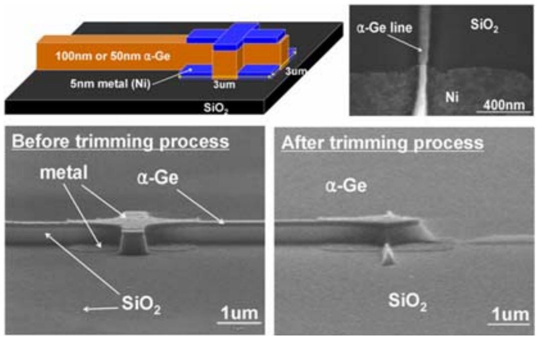


Fig. 4 Schematic and SEM images of the patterned and trimmed Ge nanowires..

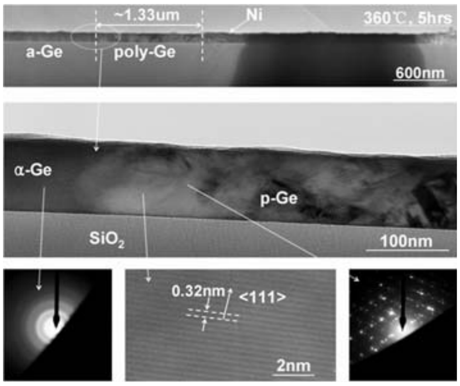


Fig. 5 TEM images and SAED patterns of 100nm thick and 70nm wide Ge wire.

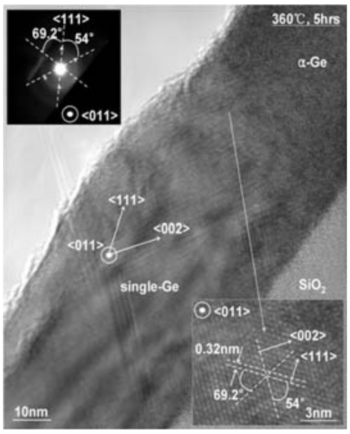


Fig. 6 TEM images and SAED pattern of 50nm thick Ge wire.

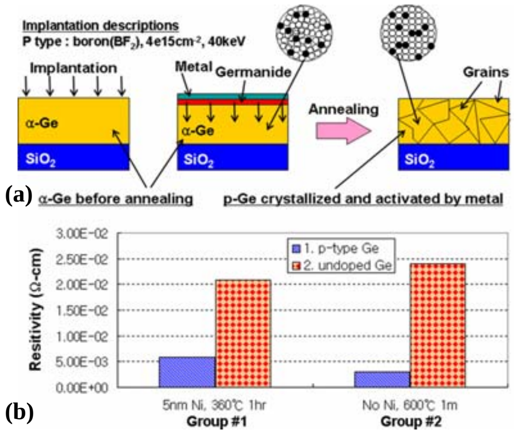


Fig. 7 (a) Schematic image for low temperature dopants activation by MIC and (b) Film resistivity of samples with and w/o Ni on p-type and undoped Ge films.

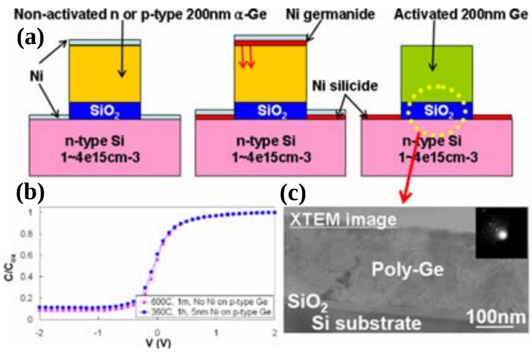


Fig. 8 (a) Schematic image for process flow of Ni-MIC Ge gate electrode Si P-channel MOSFET, (b) C-V curves, and (c) TEM image of the Ge gate electrode.

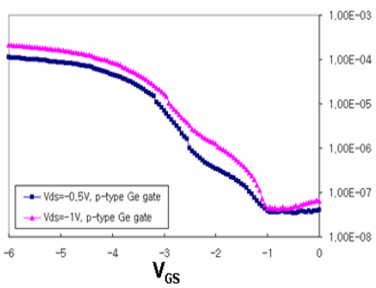


Fig. 9 Id-Vg characteristics of Si P-MOSFET with Ni-MIC Ge gate electrode.

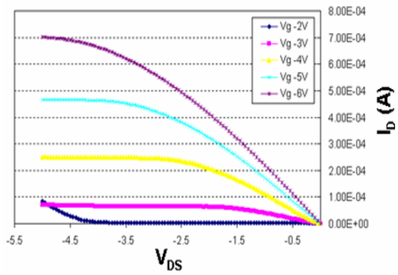


Fig. 10 Id-Vd characteristics of Si P-MOSFET with Ni-MIC Ge gate electrode.