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Narrow Trench Filled Source/Drain Contact for 3D MOSFET

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Phone: +82-53-950-6843, Fax: +82-53-950-7932, E-mail: shhahm@ee.knu.ac.kr**I. Introduction**

For the continuous CMOS scaling beyond the 32nm node, a number of fully depleted three-dimensional devices such as the FINFET, Surround Gate and TriGate had been proposed to deal with SCE [1,2]. Concerns, however, include the formation of narrow and uniform pattern while providing the low series resistance from the extension and contact regions of the device, ensuring the threshold voltage control and achieving the source/drain contact formation.

Agglomeration of silicide and leakage current of source/drain junction becomes severe in small-scale devices [3]. To resolve the problem of silicide, selective epitaxy of Si or SiGe was proposed to the source/drain contact [4]. According to ITRS 2005, 32 nm CMOS requires the low contact resistivity of $2 \times 10^{-8} \Omega \text{cm}^2$ which is hard to realize with the known contact technology. The contact resistance is a function of Schottky barrier and doping as shown in Fig. 1. Also in the 3D devices, fin corner effect is an important issue not only in the channel region but in the S/D contacts.

In this paper, we proposed a novel source/drain contact formation technique for the 3D MOSFET structures, which are also suitable for the self-aligned dual/single metal contacts and silicide contacts. And we simulated and experimentally investigated the silicide properties of source/drain contact in 3D structure.

II. Novel S/D Contact Structure for 3D MOSFET

The proposed MOSFET structure and process flow is shown in Fig. 2. It has a very narrow trench (typically 20 nm opening) between silicon fin and fin side spacer of source/drain region, which was formed by the removal etch of dielectric after formation of an extra dummy spacer (Fig. 2(a)). And we deposit the metal to fill up the narrow trench completely by atomic layer deposition (ALD) with excellent step coverage for the nano-scale and 3D structure devices [6]. Fig.2(b) and (c) are the double side metal and the tri-sided silicide contact, respectively. From the experimental results, we confirmed the metallization condition that the contact metal was filled up the narrow trench of less than 50 nm without void as shown in Fig. 3.

The proposed contact can be implemented by the self-aligned source/drain contacts, both metal contact or silicide contact. It is a prominent process to reduce the large source/drain contact resistance in the 3D MOSFET structures by the help of low sheet resistance, and low contact resistivity.

Fig. 3 shows the SEM images according to the silicidation condition. Fig.3(a) is a cross-section for a direct silicidation

after metal deposition where the silicon body has been consumed from the top. It deteriorates the aspect ratio of the 3D fin structure. Fig.3(b) is for a silicidation after removal of the top metal where only the fin sides have been consumed and better-controlled by the side metal filling into the narrow trench. The 3D devices' contact size is same with the double sides of silicided area, which may ensure the low leakage current between source and drain.

Table 1 shows the effective resistivity of the two metallization methods described in Fig.3. We measured the resistance and calculated the resistivity by using the long fin body connected by the probing contacts. The resistivity for silicidation after etching the top metal has rather low than that of three-sides contact. Measured resistance curves for various fin dimension are shown in Fig. 4.

Fig. 5 shows the simulation results of contact resistances for the two contact structures shown in the figure as (a) with both top and side contacts and (b) with only side contacts. In the wide fin, structure (a) has the lower contact resistance than that of structure (b). However, for narrower than 170 nm fin width, below which the dimension of 3D MOSFET shall be determined, structure (a) has the larger contact resistance because of the corner effects. It also supports the proposed S/D contact method is suitable for nano scale 3D-MOSFET.

III. Conclusions

We proposed a novel source/drain contact formation technique for 3D MOSFET structure, which is a simple, self aligned process. Both dual/single metal contact and silicide contact are available using the proposed technique. We investigated the silicidation cross-section and contact properties between metal and silicide S/D contacts. We also showed a simulation result which confirmed that this technique is applicable to the nano-scale devices.

Acknowledgement

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Reference

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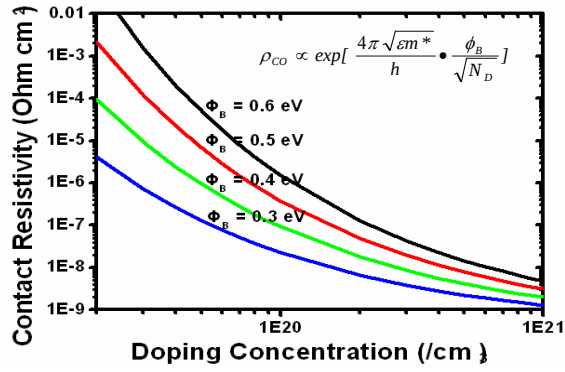
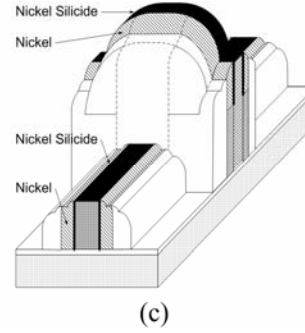
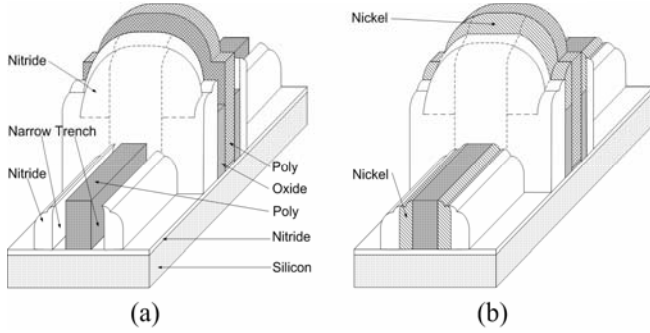


Fig. 1. Calculated contact resistance



- Fin formation
- Gate dielectric deposition
- Gate formation
- Dielectric deposition
- Spacer formation
- Dielectric etch (a)
- S/D metal filling (b,c)
- Pad metal formation

Fig. 2. Process flow of proposed contact structure

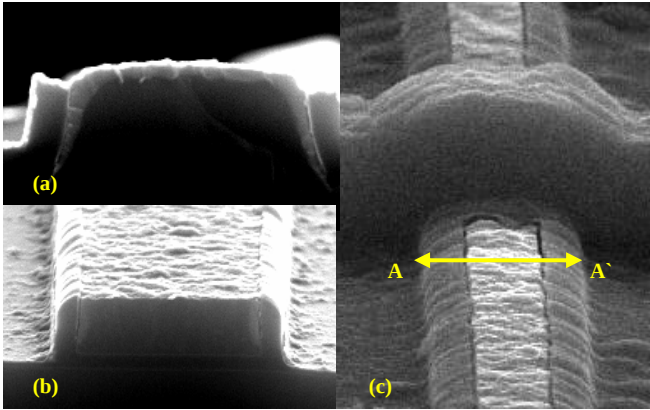


Fig. 3. SEM image of the trench contacts for (a) direct silicidation after metal deposition and (b) silicidation after removal of the top metal cutting A-A' in the fabricated MOSFET (c)

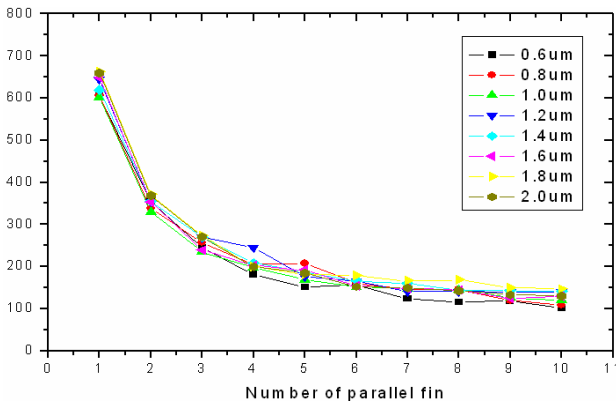


Fig. 4. Measured resistances for the silicidation after etching the top metal

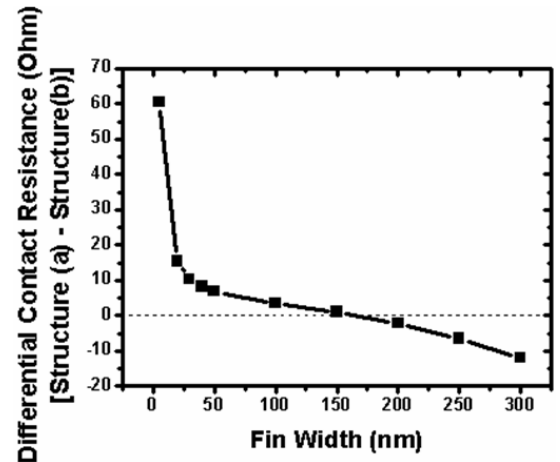
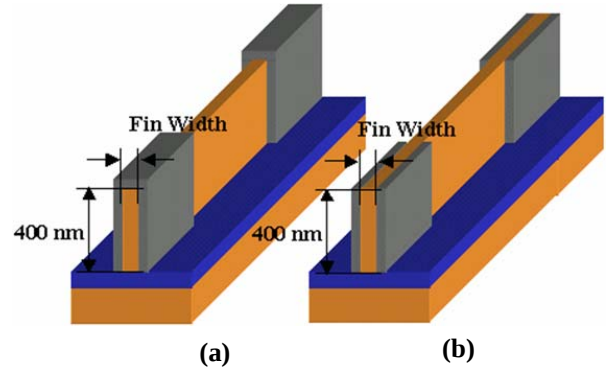


Fig. 5. Contact resistances versus fin width simulation for the two contact structures; (a) tri-side contact and (b) double side contact