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A Novel Gate Electrode Structure for Reduction of Gate Resistance of sub-0.1μm RF/mixed-signal MOSFETs

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Abstract

To reduce noise and enhance gain for scaled-down MOSFETs, a novel gate electrode structure with "Direct Finger Contact" (DFC) is proposed. The DFC structure reduces the gate electrode resistance by 40%. In spite of the increased parasitic capacitance, a maximum frequency of oscillation (f_{max}) is kept unchanged to that of the conventional MOSFETs. Because of the reduced gate resistance, a minimum noise figure, NF_{min}, is expected to decrease drastically. This structure is suitable for low-noise sub-0.1μm RF/mixed-signal SoCs.

Introduction

High gain and low noise MOSFETs are essential for RF/mixed-signal SoCs. The RF performances of MOSFETs have improved steadily as the miniaturization (Fig.1). However, increased parasitic elements such as resistances and capacitances degrade these performances. Parasitic resistances are more serious problem than parasitic capacitances for RF circuits such as low noise amplifier (LNA). Especially, a gate electrode resistance becomes a dominant problem because of the miniaturization of the gate length. The effective gate electrode resistance R_{ele} degrades gain and noise in RF circuits, while its influence on digital circuits is relatively small. For example, a minimum noise figure NF_{min} is roughly proportional to square root of R_{ele}.

To reduce R_{ele} metal-gate structures were proposed [1]. However, these structures needed complicated additional processes. "Al-shorted silicon gate structure" having a contact in an active region was also proposed [2]. This structure needed uneven gate electrode pattern which was not suitable for the sub-0.1μm lithography. In this paper, we propose a novel gate electrode structure such as "Direct Finger Contact" (DFC). By arranging contacts on a straight line gate electrode not only in the STI region but also in the active region (finger area), R_{ele} is drastically reduced. We demonstrate a DC and RF characteristics, such as cut-off frequency (f_T) and maximum frequency of oscillation (f_{max}) and R_{ele}, of the DFC MOSFETs.

Structure of Direct Finger Contact (DFC)

The top and the cross sectional views of DFC are shown in Fig.2 and 3, respectively. The gate electrode contacts wider than the gate electrode are arranged in the active region, and a local metal wire is arranged just above the gate electrode in parallel. The R_{ele} of RF MOSFETs is composed of a lateral sheet resistance and a vertical interface of a silicide electrode [3]. Because of the miniaturization of gate length L, R_{ele} of the conventional MOSFETs becomes large. On the other hand, in DFC structure, the lateral resistance becomes negligible because of the local metal above the gate electrode, which reduces the gate electrode resistance drastically. Because of the additional local metal wire and contacts, the parasitic capacitances of DFC become larger than that of the conventional one. The DFC structure, however, is effective to improve the performances of RF circuits because the parasitic resistances are more serious problem for RF circuits than the parasitic capacitances.

Fabrication of the DFC MOSFET

To evaluate the performances of the RF MOSFETs with DFC, we fabricated RF MOSFETs with multi finger structure as shown in Fig.4. The gate length L_{mask}=0.048μm, the finger width W_{finger}=1μm, the number of fingers N=20, and the number of metal layers was two. To reduce the influence of the additional parasitic capacitance arise from DFC, we fabricated various SD-pitch MOSFETs (Fig.4).

Results and Discussion

Fig.5 compares the DC drain current I_{on} of DFC and conventional MOSFETs. While the DFC has contacts penetrating stress liner, stress of MOSFETs is reduced. The degradation of I_{on}, however, was negligible for any SD-pitches and the stress liner was still effective for DFC structure.

RF characteristics were investigated by the S-parameter measurement. From the S-parameter, f_T, f_{max}, R_{ele} and parasitic capacitances were calculated [3]. Measured frequency was 1~50GHz. Fig.6 compares the parasitic capacitances of DFC and a conventional structure as a function of the SD-pitch. It is shown that when the SD-Pitch becomes wide, an additional parasitic capacitance of DFC becomes negligible. Fig.7 shows f_T as a function of the gate bias V_G. Because of the increased parasitic capacitance, f_T of DFC was smaller than that of the conventional one, but degradation of f_T was relieved at wide SD-pitch as shown in Fig.8. Fig.9 and 10 show f_{max} as a function of V_G and f_{max} as a function of the SD-pitch. The f_{max} of DFC was almost equal to that of the conventional one in spite of the degraded f_T. This is because f_{max} of DFC is owing to the reduction of R_{ele}.

Next, R_{ele} was estimated by using the theoretical equation [3]. Fig.11 shows the extracted R_{ele}. Over 40% gate resistance reduction was observed to that of the conventional one, indicating that the DFC structure is effective to reduce gate electrode resistance R_{ele}. The NF_{min} was calculated by the SPICE simulator using measured parameters. Table.1 compares the measured characteristics of DFC and the conventional MOSFETs. Because of the reduction of R_{ele}, 20% reduction of NF_{min} was estimated.

Conclusions

Direct finger contact structure (DFC) was proposed to reduce the gate electrode resistance of sub-0.1μm RF/mixed-signal MOSFETs. By arranging the gate electrode contact in the active region, the gate electrode resistance was reduced by 40%. The increased parasitic capacitance of DFC degrades f_T, but f_{max} of DFC was as large as that of conventional MOSFETs because of the reduction of the gate electrode resistance. As a result, the minimum noise figure was expected to decrease drastically. This DFC structure is suitable for sub-0.1μm RF circuits to reduce noise and enhance gain.

Acknowledgement

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References

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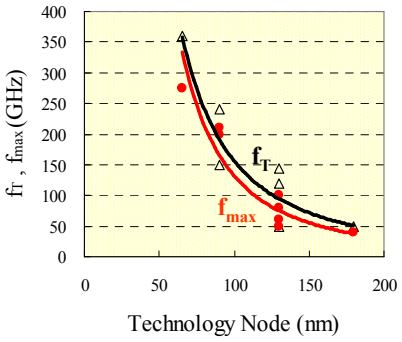

Fig.1 Technology trend of f_T , f_{max}.
The RF performances of MOSFETs have improved steadily as the miniaturization.

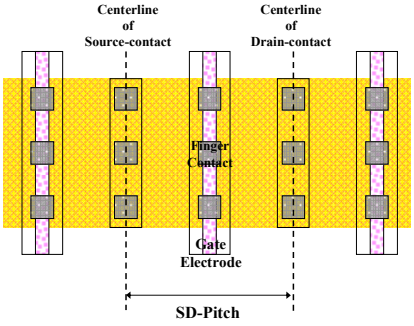

Fig.4 Top view of the multi-finger MOSFET.
SD-pitch is defined as the distance between the source electrode and the drain electrode.

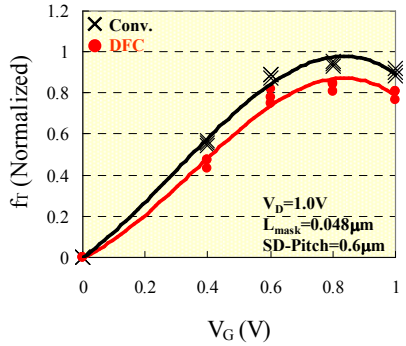

Fig.7 Dependence of f_T on the gate bias V_G.
The maximum value of f_T is normalized to 1.
f_T of DFC structure is smaller than that of the conventional one because of the increased parasitic capacitances.

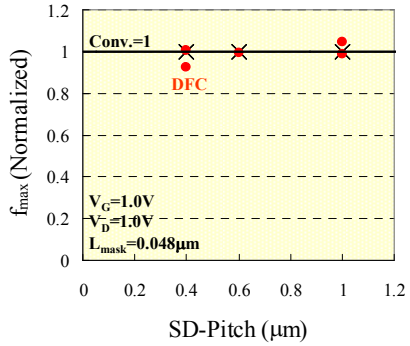

Fig.10 Dependence of f_{max} on the SD-pitch.
f_{max} of the conventional MOSFETs is normalized to 1. f_{max} of DFC and the conventional MOSFETs are almost equal at any SD-pitches.

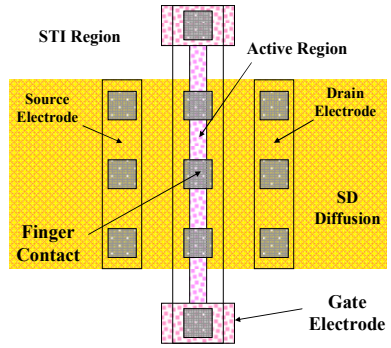

Fig.2 Top view of DFC structure.
Finger Contacts are arranged in an active region.

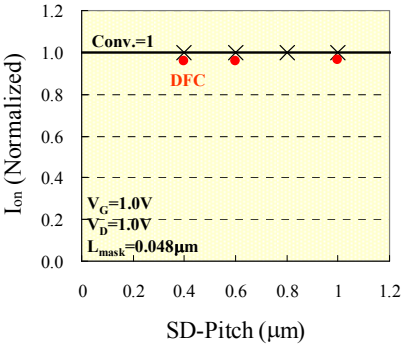

Fig.5 Dependence of the DC drain current I_{on} on the SD-pitch. I_{on} of conventional MOSFETs is normalized to 1. A degradation of I_{on} of DFC is negligible at any SD-pitches.

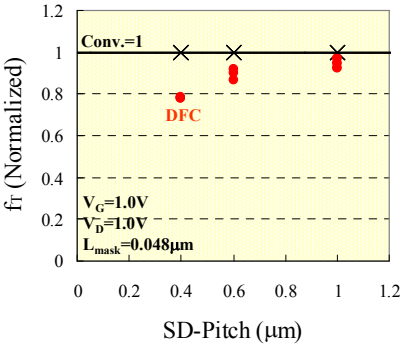

Fig.8 Dependence of f_T on the SD-pitch.
f_T of the conventional MOSFETs is normalized to 1.
When the SD-pitch becomes wide, f_T of DFC approaches that of the conventional MOSFETs

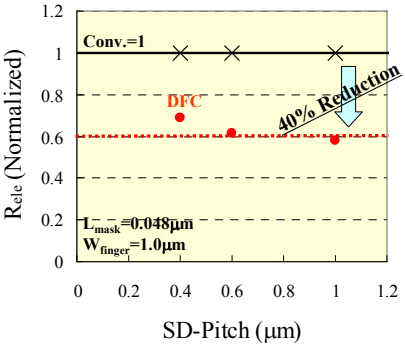

Fig. 11 Dependence of Gate electrode resistance on the SD-pitch. R_{ele} of the conventional MOSFETs is normalized to 1. Gate electrode resistance is independent of the SD-pitch.
The gate electrode resistance of DFC was reduced by 40%.

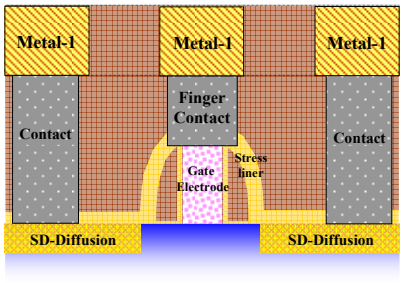

Fig.3 Cross sectional view of DFC structure.
Finger Contacts, wider than gate electrode, are arranged with penetrating the stress liner.

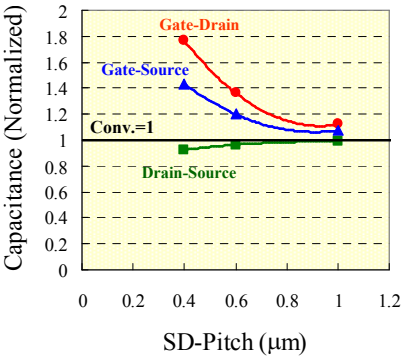

Fig.6 Dependence of parasitic capacitance on the SD-pitch. The capacitances of the conventional MOSFETs are normalized to 1. The additional capacitances, gate-drain (circle), gate-source (triangle) and drain-source (square), of DFC structure become small as SD-pitch becomes wide.

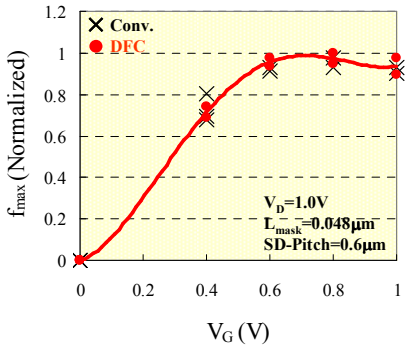

Fig. 9 Dependence of f_{max} on gate bias V_G.
The maximum value of f_{max} is normalized to 1.
f_{max} of DFC is as large as that of the conventional MOSFETs

Table.1 Characteristics of DFC and conventional MOSFETs (V_G=V_D=1V, SD-pitch=0.6μm).
The values of the conventional MOSFETs are normalized to 1. NF_{min} was calculated by the SPICE simulator using measured parameters.

	Conventional	DFC
I_{on}	1	- 5%
f_T	1	- 13%
f_{max}	1	1
Gate resistance	1	**- 40%**
NF_{min} (Simulated)	1	**- 20%**