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A Fundamental Study Toward the Realization of an SPRAM-based Low Power FPGA

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I. Introduction

Magneto-resistive Random Access Memory (MRAM) is a nonvolatile memory exhibiting excellent characteristics such as high speed operation, high density, and high endurance [1]. The use of MgO barrier in Magnetic Tunnel Junction (MTJ) [2] improves the read operation performance remarkably. However, the conventional MRAM consumes much power in the write operation, because it uses current induced magnetic field for the operation. To overcome this problem, spin torque transfer magnetization switching was demonstrated [3], [4]. This approach also improves the writing selectivity, because the writing current passes through the MTJ directly. The excellent reading/writing performance, low power consumption, and nonvolatile characteristics of such a SPin-transfer torque RAM (SPRAM) can be applied for the configuration memory for reconfigurable devices.

FPGA (Field Programmable Gate Arrays) logic circuit, which is a representative of reconfigurable devices, has been developed in the last twenty years. Figure 1(b) represents a logic block of a conventional FPGA. The FPGA circuit uses SRAM as an intermediate memory; however SRAM is volatile, which means that all the logic functions must be pre-programmed at each power-up and external PROM (Programmable ROM) is necessary. Internal flash memory is now used to replace the external memory. However, the number of writing cycles is finite, and thereby it cannot be used as the intermediate memory.

In this paper, the authors propose the improved logic block construction of FPGA shown in Fig. 1(a). Configuration memories used in the conventional FPGA are replaced with SPRAM. Implementation area decreases and the logic block does not need any external nonvolatile memory. Moreover, supply voltages of memory cells except working cells are suppressed by a power control, because SPRAM does not need any power supply for keeping logical information. The integration of SPRAM in FPGA also allows the logic block to rapidly configure the logic functions and easily realize the dynamical reconfiguration.

II. Configuration of a logic block with SPRAM and its readout characteristics

Figure 2 illustrates a block diagram of two-inputs logic block with SPRAM. It consists of a SPRAM cells block, a two-inputs Look-Up Table (LUT), and an output flip-flop. The SPRAM cells block consists of 4 bit SPRAM cells, an SA (Sense Amplifier), an SPRAM reference cell, and a write circuit. Figure 3(a) shows an SPRAM cell circuitry, which consists of an MTJ device, a selecting transistor, a Word Line (WL) and Bit Lines (BLs). An MTJ resistance, which represents the stored logic, changes when the applied current, which through the MTJ, over the threshold current as shown in Fig. 3(b). The MTJ resistance depends on the applied direction. Figure 4 represents a two-stages sense amplifier. The first stage is a current-mode sense amplifier that senses the amount of MTJ current. The second one is a voltage-mode sense amplifier that outputs a digital value. The SPRAM reference cell consists of four MTJs as represented in Fig. 5. This cell generates the intermediate MTJ resistance of $(R_{ap} + R_p)/2$. The write circuit is a pass gate logic circuit controlled by the select signals. Readout or write operation is selected by R/W, and the write data from SRAM or from external is selected by WB/EX. The two-inputs LUT is composed of a 2 bit selector and 4 bit SRAM cells. Combination of input signals (InH and InL), and data that stored in SRAMs implements arbitrary logic function.

HSPICE simulation has been applied with BSIM3 level 49 model parameter. Figures 6(a) and 6(b) show the readout simulation result of the four-inputs LUT and D-FF, and SA, respectively. These figures show that the proposed circuit is successfully operated.

III. Conclusions

Improved logic block with SPRAM was proposed and the readout characteristics were simulated in this paper. The high speed readout operation was confirmed. This circuitry is now prototyping with CMOS 0.14 μm technology.

References

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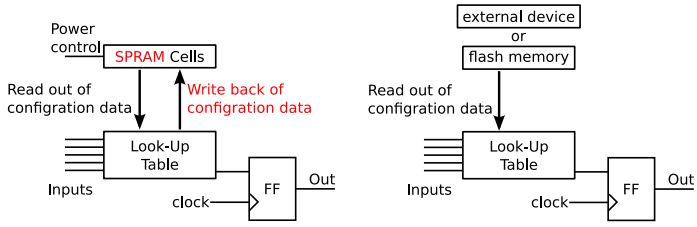


Fig. 1. Comparison of improved logic block with conventional one: (a) SPRAM-based FPGA; (b) conventional FPGA.

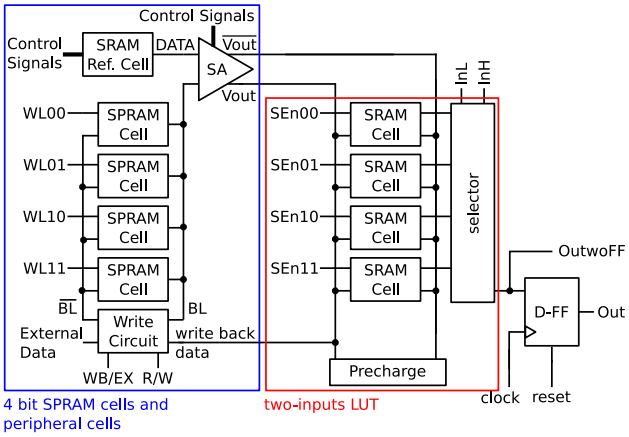


Fig. 2. Block diagram of two-inputs logic block with SPRAM.

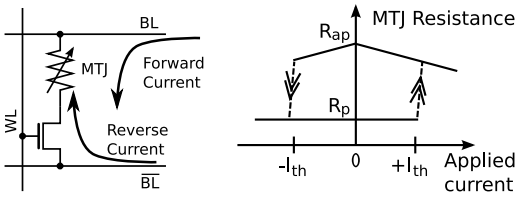


Fig. 3. (a) SPRAM cell circuitry and (b) its I-R characteristic ($R_p = 1$ kΩ, $R_{ap} = 3$ kΩ, $I_{th} = 200$ μA).

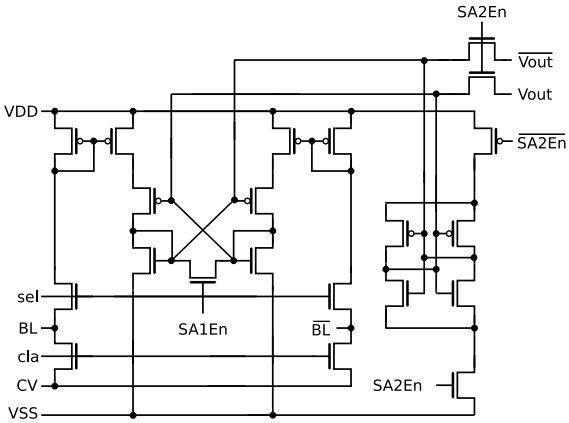


Fig. 4. Sense amplifier circuitry.

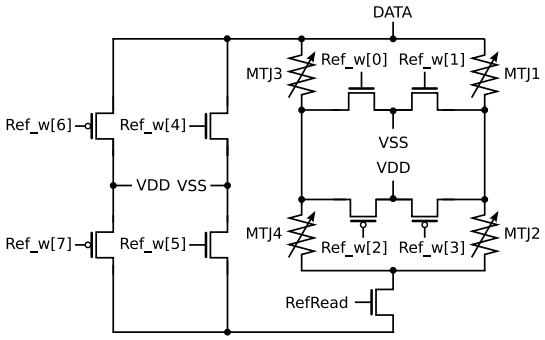
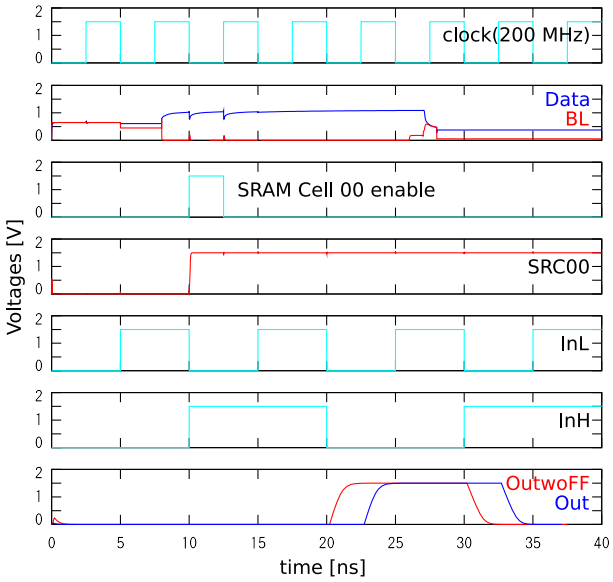


Fig. 5. SPRAM reference cell circuitry.



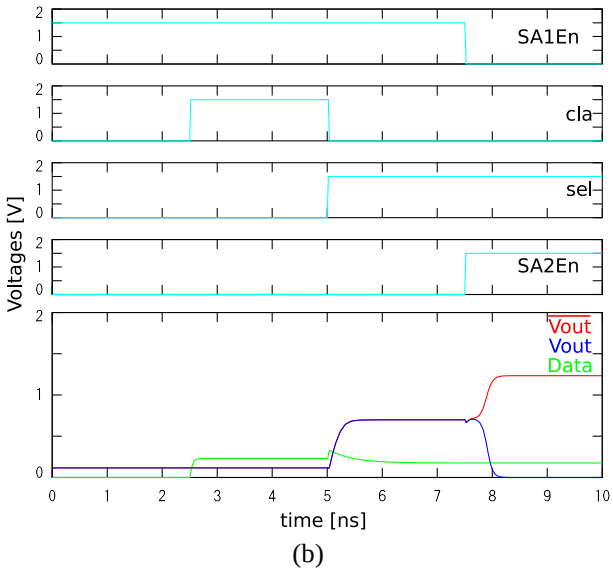


Fig. 6. Simulation results with clock frequency is 200 MHz and power supply is an 1.5-V: (a) time series of two-inputs LUT and D-FF simulation with MTJ is 3 kΩ (logical “1”); (b) time series of SA simulation with MTJ is 3 kΩ (logical “0”).