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Plasma Physics for Reducing PID in Nano-structure Patternings

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1. Introduction

In the last two decades, various kinds of plasma damage have been known to occur during low temperature plasma processes in the trend toward the miniaturization of ULSI circuits. Charging damage in the fabrication of a nanoelectronic device is one of the electrical damages during plasma etching and is caused basically by a huge difference of the flux velocity distribution $\Gamma(v) = vg(v)$ between positive ions and electrons toward the wafer to be processed. The difference in $\Gamma(v)$ is essential for both metallic and dielectric wafer, subject to the ambipolar diffusion in a time-averaged fashion, interacting with the electron-ion plasma[1].

With the evolution of the technology node, charging damage will increase due to several factors, increase of plasma exposure time, decrease of annealing temperature, and narrow process window, etc., The progress of a top-down nanotechnology depends on the development of in situ diagnostics and of the prediction tool for plasma damage to lower-level elements, and on the development of charging-free plasma process.

In this talk, we review the in situ charging measurements by using a test chip both in conventional operation and in the negative charge injection on the wafer exposed to the plasma etching together with optical emission spectroscopy [2,3]. Next we show the characteristics of the charging potential on the bottom of SiO_2 holes during etching in a two-frequency CCP, and we refer to the procedure to reduce the bottom potential utilizing the negative charge injection to the hole bottom under the artificial formation of a double-layer close to the wafer. In addition, the saturated characteristics of the bottom charging voltage are experimentally estimated from a static breakdown based on the local charge separation on the dielectric [4]. Finally the feature profile evolution during plasma etching is predicted in 2f-CCP by using VicAddress, vertically integrated computer aided design for device processes [5].

2. Experimental arrangement

The experimental 2f-CCP reactor for etching is described in detail in addition to the electrical and optical procedure [2,3]. Figure 1 shows a schematic diagram of the reactor for SiO2 etching and the measurement system for the charging potential on the test-hole bottoms relative to the flat Si and for the CT image of the OES in the interface between the bulk plasma and wafer. The powered electrode is driven at VHF, 100 MHz. The VHF source is operated both in CW and in a pulsed mode with an on/off period of 10 us. The bias electrode is also operated by the CW mode and a pulse with single positive component (SPC) of 0.7 us width at LF, 500 kHz at 25 mTorr and 50 sccm in Ar and CF4(10%)/Ar. VHF and LF voltage waveforms in the 2f-CCP are synchronized at the zero-crossing phase from the negative to positive in the pulsed cycle of the VHF source. The dc self-bias voltage is kept almost constant even at the pulsed mode of the LF-bias voltage.

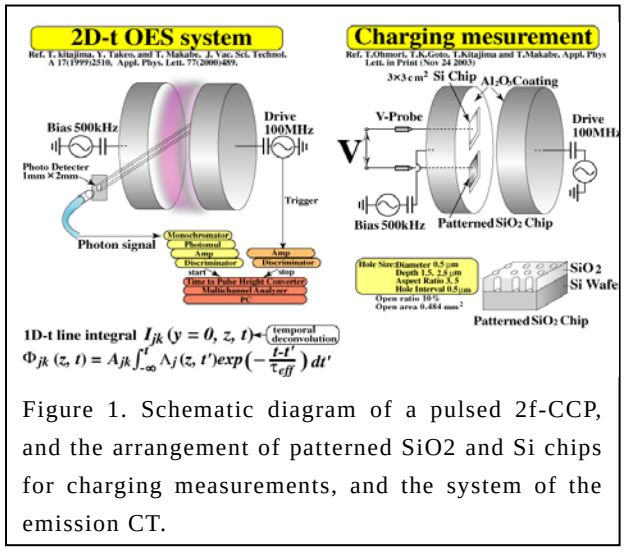

Figure 1. Schematic diagram of a pulsed 2f-CCP, and the arrangement of patterned SiO2 and Si chips for charging measurements, and the system of the emission CT.

3. Plasma structure and charging

In the plasma etching of SiO2, the essential point is a preparation of “passive sheath” in front of the strongly biased-wafer in order to produce high energy ions, and the function is relevant to the plasma source at VHF. The passive sheath performs the irradiation of the positive ion beam and the shower of radicals to the wafer. In a

dielectric etching, the pair of fluxes, positive ions and electrons, becomes a basic issue as the local surface charging. A new and basic technology is expected to accelerate negative charge to the wafer. Figure 2 shows the experimental result of the injection of negative charges to the wafer in CF4(10%)/Ar. As a result, at appropriate phase of the external bias pulse (SPC), the bottom charging potential trends to be cancelled. Attention will be paid to the results of pure Ar in Fig. 3. It implies that negative ions play a key role in the charge cancellation.

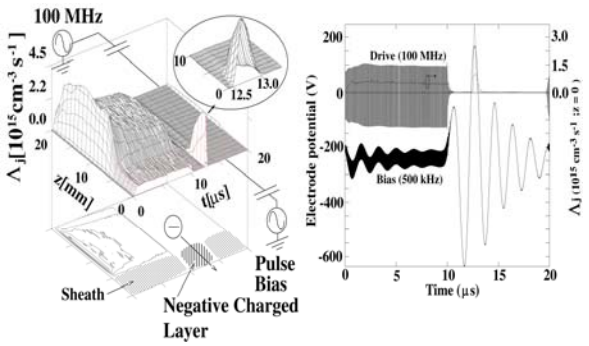

Figure 2. Axial net excitation rate of Ar(2p1) under the bias pulse (SPC) at 12.5us. The wafer is located at z = 0. The amplitude of the SPC is 400 V.

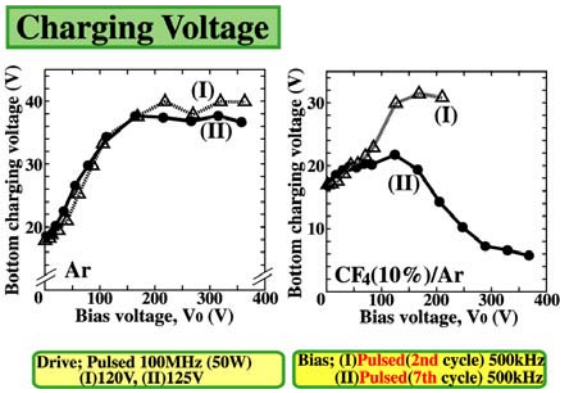

Figure 3. Charging voltage on a contact hole bottom at AR = 5 as a function of bias amplitude in Ar (a) and CF4(10%)/Ar (b). The bias pulse (SPC=0.7us) is applied at 3 us (I) or 12.5 us(II) during the on/off period (20 us) of the VHF.

The double layer formation close to the wafer exposed to plasma etching is the origin of the negative charge injection. In fact, Figure 3 shows the depletion of the bottom charging in CF4(10%)/Ar. The saturation characteristics in Ar in Fig. 3 are reproduced on the wafer having a shower of charges in vacuum (see Figure 4).

Feature profile evolution will be predicted under the circumstances among charging, etching and deposition by considering the basic processes on the wafer interacting with plasmas. Some of predictive images will be shown.

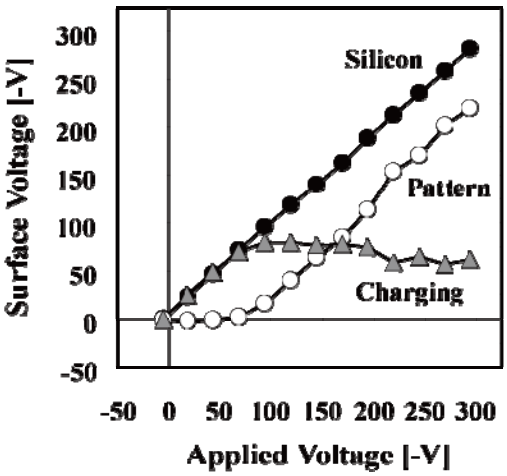

Figure 4. Charging voltage on a contact hole bottom at an AR = 5 as a function of accelerating voltage of electrons in vacuum. The test chip of SiO_2 consists of 2.3 x 10^{10} holes of 300 nm in diameter.

References

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