Low-k Impact on Circuit Performance Demonstrated in High-Speed LSIs

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Abstract: Low-k impact on circuit performances is investigated in high-speed 65nm-node CMOS LSIs with 11-layered Cu dual-damascene (DD) interconnects. Three types of local low-k/Cu structures (M2-M5) with Keff=3.4, 3.1 and 2.9 are compared in terms of the circuit performance. The interline capacitance (C\(_{\text{int}}\)) is reduced by 12% from Keff=3.4 to 2.9. NAND-type ring-oscillators (ROSCs) with the 100um-long interconnect load demonstrates that the lowest Keff structure reduces the signal delay and the power consumption by 12.1% and 10.2% in GHz-range oscillation, respectively. The 2GHz SRAM with Keff=2.9 reveals 4.0% reduction in the bit-line capacitance (M2), resulting in 5.8% improvement of \(V_{\text{dmin}}\) or essentially widening the operation margin.

Introduction

To improve LSI performance, low-k dielectrics, such as rigid-SiO\(_2\) (k=3.1), porous-SiO\(_2\) (k=2.7) and molecular-pore-stacking (MPS) SiO\(_2\) (k=2.5) \(^1\), have been implemented into the Cu-interconnects in 90nm, 65nm and 45nm-node, respectively. In this work, in order to clarify the low-k impact on the circuit performance, three types of local interconnect structures of Keff=3.4, 3.1 and 2.9 are compared in a 65nm-node high-speed CMOS LSI with 11-layered Cu DD interconnects (Fig.1). Basic circuit performance is evaluated by using the NAND-type ROSC in GHz-range oscillation and high speed 2GHz SRAM in the full integration chips (Fig.2).

Experimental

A 65nm-node CMOS LSI with \(L_g=40\)nm and Ni-silicide were used for the test-vehicle. Three types of low-k structures were implemented into the local Cu DD interconnects of M2-M5. In BEOL-A (Keff=3.4), porous-SiO\(_2\) (k=2.7) inter-metal-dielectics (IMD) with a SiO\(_2\) hard-mask (HM) was stacked on the rigid-SiO\(_2\) (k=3.1) via-ILD with a SiO\(_2\) etch-stop-layer (ES). In BEOL-B (Keff=3.1), MPS-SiO\(_2\) (k=2.5) with rigid-SiO\(_2\) HM (k=3.1) was stacked directly on the rigid-SiO\(_2\) via-ILD (k=3.1). In BEOL-C (Keff=2.9), the porous-SiO\(_2\) (k=2.7) was introduced to the via-ILD. From M6 to M9, rigid low-k (k=3.0) was used as semi-global lines, and SiO\(_2\) was used in M10 and M11 as global lines. Critical dimension (CD) in the DD trenches was well controlled by via-first multi-resist-mask process.

Results and Discussion

The CMOS performances such as \(V_{\text{gs}}I_{\text{ds}}\) and \(I_{\text{ds}}\) were not affected by the low-k integration (Fig. 3). Selective etching of the C-rich MPS-SiO\(_2\) IMD to the Si-rich non-porous or porous SiO\(_2\) ILSDs reduced the distribution of trench depths in BEOL-B and -C without ES. These processes accomplished tight distributions of the line resistance and the via-resistance in each interconnect structure (Fig.4). The line capacitances of 200nm-pitched M4 lines in Keff=2.9 were reduced by 12% referred to that in Keff=3.4 with keeping the same line resistance (Fig.5). To improve the adhesion between IMD and HM, the IMD surface was treated by He-plasma. The plasma power and the time duration, or essentially the plasma energy, were carefully minimized to reduce the interline leakage current especially for BEOL-B and -C. The the trap potential, associated with the interline leakage in Poole-Frenkel emission model, was estimated to -0.8eV irrespective of the He-plasma energy. The \(C_{\text{pl}}\) on the other hand, decreased with the He-plasma energy, implying that suppression of the leakage current is originated from decrease in the defect density at the interface of HM/IMD (Fig.6). The TDDB lifetime in the lowest defect condition was well fitted in E-model with the parameters of \(\text{Ea}=0.78eV\) and \(\gamma=5.1,\) leading to estimated lifetime longer than 10 years (Fig.7).

The basic circuit performance was evaluated by the NAND-type 25-stage ring-oscillator (ROSC) with interconnect loads of a 200nm-pitch and 100um-long lines. The high oscillation frequency in >2GHz was measured through 6-stage frequency divider. The signal propagation delays (\(\tau_{\text{pl}}\)) at 1.0V reduced by 12.1% in Keff=2.9 (Fig.8). Dynamic power per cycle, in which the standby-power was subtracted from the active-power, dropped by 10.2% in Keff=2.9 (Fig.9). It is confirmed that the low-k realizes not only the high speed operation but also the low power operation in GHz-range operation.

Bit-line capacitance of M2 in 2GHz SRAM decreased by 4% in Keff=2.9 referred to Keff=3.4 (Fig.10). The minimum power supply voltage in the SRAM macro operation, \(V_{\text{dmin}}\) was evaluated for the chips selected through several test sequences. Reduction of \(V_{\text{dmin}}\) was clearly confirmed from 0.68V to 0.64 V (~5.8%) at 0% probability by the Keff reduction from 3.4 to 2.9 (Fig.11), meaning expansion of the operation margin. Low-k films were effective for improving the high speed SRAM performance (Table.1).

Conclusion

Low-k impact on circuit performance was investigated by using high-speed 65nm-CMOS LSI. Introduction of MPS-SiO\(_2\) IMD/porous-SiO\(_2\) via-ILD (Keff=2.9), reduced the interline capacitance by 12%, referred to Keff=3.4. Reductions of the signal delay and the power consumption of ROSC was confirmed in the actual GHz-range operation. In the high-speed 2GHz SRAM, 4% reduction in the bit-line capacitance widened the operation margin such as 5.8% improvement of \(V_{\text{dmin}}\). The low-k introduction is a key to the low power and high performance operation.

Fig. 1 A cross-sectional TEM photograph of 11-layered Cu dual damascene (DD) interconnects for 65nm-node high-end ULSI, demonstrating MPS-SIOCH films (k=2.5) in the local lines of M2-M5 with Keff=2.9.

Fig. 2 Schematic illustrations of the local Cu DD interconnects with Keff=3.4 (BEOL A), 3.1 (BEOL B) and 2.9 (BEOL C). The circuit performances in ROSC and high-speed SRAM were evaluated after full integration with 11-layered Cu interconnects.

Fig. 3 Ids-Vgs characteristics of NMOS and PMOS at |Vds|=0.05V and 1.0V.

Fig. 4 Distributions of line and via resistances in Cu interconnects.

Fig. 5 Rint-Cint of M4 interconnects in BEOL A (Keff=3.4), B (Keff=3.1) and C (Keff=2.9).

Fig. 6 Low filed conductivity and depth of trap potential estimated by Poole-Frenkel emission.

Fig. 7 TDDB lifetime estimation as a function of the interline electric field.

Fig. 8 Distributions of propagation delay in ROSC with 100μm-long M4-lines at 1.0V.

Fig. 9 Dynamic power per cycle in NAND-type ROSC as a function of Keff.

Table 1 Summary of Low-k impact

<table>
<thead>
<tr>
<th>Symbol</th>
<th>BEOL A</th>
<th>BEOL B</th>
<th>BEOL C</th>
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<tr>
<td>Keff</td>
<td>3.4</td>
<td>3.1</td>
<td>2.9</td>
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<tr>
<td>Line resistance (Ohm/μm)</td>
<td>0.17</td>
<td>0.17</td>
<td>0.17</td>
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<tr>
<td>Line Capacitance (fF/μm)</td>
<td>168</td>
<td>153</td>
<td>148</td>
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<td>via resistance (Ohm)</td>
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<td>2</td>
<td>2</td>
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<td>Signal delay (ns)</td>
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<td>ROSC Dynamic power (μW/unit)</td>
<td>100</td>
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<td>SRAM (VDDmin)</td>
<td>0.68V</td>
<td>0.65V</td>
<td>0.64V</td>
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