Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 722-723

C-6-4

Dielectric reliability of 50nm ½ pitch structures in Aurora® LK

S. Demuynck*, H. G. Kim**, C. Huffman, M. Darnon, H. Struyf, J. Versluijs, M. Claes, G. Vereecke, P. Verdonck, H. Volders, N. Heylen, K. Kellens, D. De Roest***, H. Sprey*** and G. P. Beyer

IMEC, Kapeldreef 75, B-3001 Leuven (Belgium)
* Phone: +32-16-28.10.06, Fax: +32-16-28.12.14, E-mail: Steven.Demuynck@imec.be
** Samsung affiliate at IMEC
*** ASM Belgium

Abstract

The dielectric reliability of Aurora® LK (k=3.0) material has been evaluated on a 50nm ½ pitch test structure. These were fabricated using a double patterning scheme and TiN MHM. The introduction of a suitable post-etch residue removal step and close-coupled processing between Cu electroplating and CMP were found to be key for achieving high yield. The median TDDB lifetime of the integrated dielectric exceeds 10yrs at typical operating voltages in memory devices.

Introduction

The ITRS roadmap indicates the need for a 3.1-3.4 effective dielectric constant material to be integrated at 50nm M1 ½ pitch in 2009 for memory-based applications [1]. While the required dielectric constant of the interlevel dielectric material is not as low as compared to logic device manufacturing, typical operating voltages are significantly higher. For that purpose, long-term dielectric reliability at higher operating voltages on 50nm ½ pitch is investigated for Aurora LK, a low porosity k=3.0 material.

Integration of yielding 50nm ½ pitch structures

Structures were fabricated in a stack of 120nm Aurora LK deposited on a 5nm SiCN/25nm SiCO liner in an Eagle12® dielectric deposition tool. A double patterning scheme was adopted using 30nm TiN metal hard mask (MHM), as described in Fig. 1 [2]. For this purpose the design was split into two parts, referred to as M1A and M1B. First 75nm M1A trenches were defined in the resist by using 193nm dry lithography on an ASML1250 scanner and a Relacs® coat and bake step was performed to shrink to 50nm dimensions in resist. This pattern was then transferred into the MHM by using a Cl-based BARC/MHM etch chemistry. N_2/H_2 based ash was used to remove remaining BARC/resist. This step was immediately followed by a short 0.17% HF wet clean to avoid corrosion of the hard mask. Subsequently the M1B pattern was printed on the M1A MHM topography, planarized by a BARC layer, aligned to the previously defined M1A layer. After transfer of the M1B photo into the MHM and again N_2/H_2-based resist ash, the dielectric etch of both M1A and M1B features in Aurora LK was performed using a $Ar/CF_4/O_2$ chemistry. The introduction of O_2 was found to be necessary to control the build-up post-etch residues and avoid etch stop in the low-k.

The remaining polymer residues, that were preferentially formed on the sidewall of the TiN MHM were not successfully removed by a 0.17% HF clean performed at 45°C in a single wafer tool. This compromised the capability to metalize 50nm trenches void-free, resulting in poor yield reflected in high sheet resistance (Rs) and large within-wafer non-uniformity (Fig. 2). Two polymer removal schemes were identified to overcome this issue, enabling high yield at 50nm ½ pitch. Scheme 1 involved a two-step clean operation consisting of a 0.17% HF clean followed by removal of the TiN MHM and the associated polymers on its sidewall by an additional inorganic clean performed at room temperature in the same single wafer cleaning tool. The other scheme involved the use of 2 commercially available aqueous organic acids (A and B) in a single wafer spin tool at 45°C. Both (A an B) leave the MHM intact after patterning. These 2 schemes result in comparable yield on the 50nm wide/1cm long M1A meander structure for organic acid A and HF/inorganic clean and slightly lower yield for organic acid B (Fig. 2).

Trenches were metalized using a 3nm PVD TaN/Ta barrier, 20nm PVD Cu seed and 500nm ECP-Cu followed by a 30sec 180°C anneal step and CMP. The CMP step removes the MHM in case the HF/organic clean scheme is chosen for post-etch residue removal. A representative TEM image of the integrated structure for the HF/inorganic scheme is shown in Fig. 3 indicating the M1A trench is smaller and patterned slightly less deep than M1B, making it the most challenging for polymer clean-up & metallization .

Delay time between the Cu electroplating and CMP step was found to be detrimental for yield and Rs uniformity through the appearance of voids spanning the 50nm trenches, either interrupting the Cu lines or effectively reducing the Cu cross-sectional area (Fig. 4). The voids, seemingly organized along grain boundaries of the Cu overburden, can be avoided by closely coupling ECP and CMP steps, indicating that the possible root cause for this issue relates to an non-optimized plating chemistry (impurities) and/or anneal condition. By performing time-critical processing for the ECP/CMP steps yield-killing voids could be avoided.

Dielectric reliability of 50nm ½ pitch structures

Dielectric reliability was evaluated on a 1cm 50nm ½ pitch M1A meander/M1B fork structure for the aforementioned post-etch polymer removal schemes at 100°C. I-V sweep measurements indicate the structures break down at voltages > 20V (or 4MV/cm) for both schemes (Fig. 5), with slightly higher values reported for organic acid A. For organic acid B values are slightly below 20V. Time-dependent dielectric breakdown (TDDB) measurements indicate similar performance at experimental conditions for both routes (Fig. 6). We used the most conservative model (E-model) to extrapolate lifetime to lower operating voltages. Extrapolations are to be taken with some caution due to relatively large confidence bounds on the voltage acceleration and lifetime distribution parameters. They indicate the 10yrs median lifetime is exceeded at voltages of 7.6V and 2.0V for the HF/inorganic clean scheme and the clean with organic acid A respectively (Table 1), indicating the potential of integrated Aurora LK to endure the high operating voltages in memory based circuits.

Conclusions

50nm ½ pitch structures were successfully integrated into Aurora LK using a MHM based double patterning scheme. Patterning was challenged by the need for an optimized etch/ash/clean combination for effective removal of polymer residues in 50nm trenches. For metalization time-critical processing was required to avoid yield killing defects revealed after CMP. The median TDDB lifetime of the integrated dielectric meets the 10yrs lifetime spec at operating voltages, typically used on memory devices.

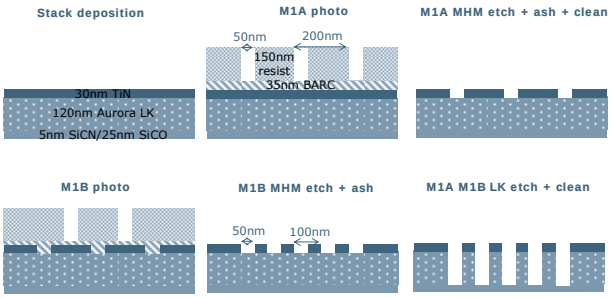

Fig. 1: Description of the double patterning processing sequence to obtain 50nm ½ pitch structures in Aurora LK.

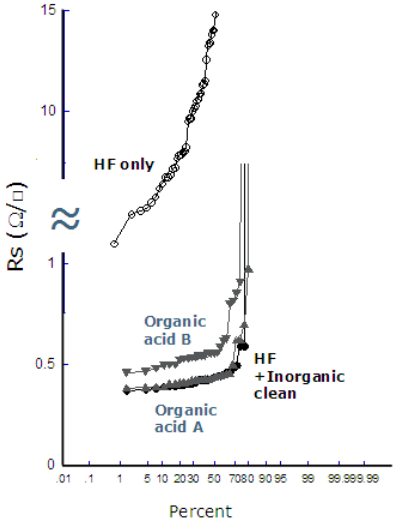

Fig. 2: Comparison of sheet resistance (Rs) and yield on 1cm 50nm ½ pitch M1A/M1B meander/fork on 4 routes for post-etch residue removal: 0.17% HF only, 0.17% HF + inorganic clean and clean with organic acid A or B.

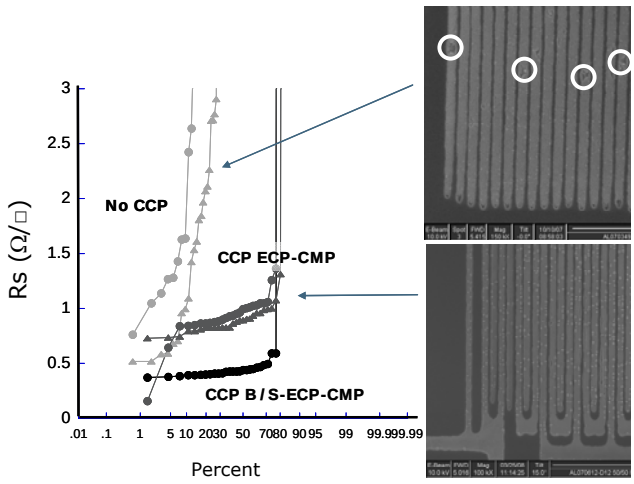

Fig. 4: Comparison of metallization performance and yield on a 1cm long 50nm ½ pitch M1A/M1B meander/fork for integration with "No CCP" (=no close-coupled processing in metallization), no delay between barrier/seed deposition, electroplating and CMP ("CCP B/S-ECP-CMP") and no delay between ECP & CMP ("CCP ECP-CMP"). In case ECP & CMP are decoupled, yield killing defects are observed after CMP. In all cases MHM was removed after etch by HF/inorganic clean.

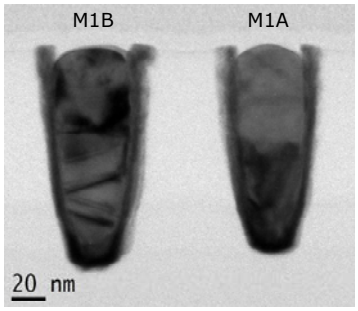

Fig. 3: X-TEM of M1A & M1B 50nm trenches after full integration where HF/inorganic clean is used as post-etch residue removal step.

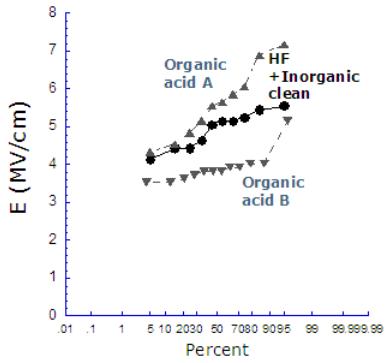

Fig. 5: Breakdown field distribution as measured at 100°C on a 1cm 50nm ½ pitch M1A/M1B meander/fork for 2 schemes for post-etch residue removal either involving MHM removal at etch (HF/inorganic clean) or MHM removal at CMP (organic acid A and B).

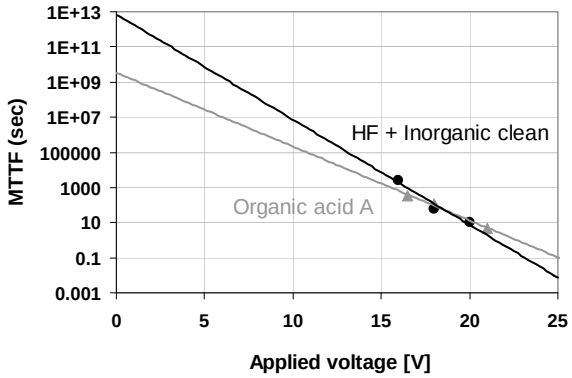

Fig. 6: E-model based TDDB lifetime extrapolation for the median-time-to-failure as evaluated at 100°C on a 1cm 50nm ½ pitch M1A/M1B meander/fork for HF/inorganic clean and organic acid A used for polymer removal.

Table 1: Voltage corresponding to 10yrs MTTF + the associated parameters describing the lifetime distribution (sigma) and voltage acceleration (a1)

Split	V (10yrs MTTF)	sigma	a1
HF+Inorganic clean	< 7.6V	2.6 (+0.62, -0.42)	-1.4 (+0.25, -0.25)
Organic acid A	< 2.0V	2.4 (+0.58, -0.42)	-0.95 (+0.10, -0.10)

References

[1] ITRS2007 roadmap
[2] J. Van Olmen et al, AMC Proc. (2007)