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An Efficient Modeling Technique with Q-curve Analytic for Design Automation

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1. Introduction

The development of high performance, low-cost CMOS technologies is a driving force behind the realization of single chip solutions for the wireless market. However, the design of integrated spiral inductors continues to hinder the advancing growth of RFIC SoC [1]. In order to promote the implementation of integrated inductors, a compact scalable physical model that accurately predicts inductor behavior with inductor geometries and processes technologies would be a useful tool for rapid spiral inductor design and optimization. In this paper, we propose a compact model that uses closed-form formulae to quickly characterize planar inductors. In addition, a systematic design methodology for spiral inductor design automation is also demonstrated.

2. Spiral Inductor Model and Quality Factor

Our compact inductor model is based on the frequency dependent twelve-element model showed in Fig. 1. The model with closed-form expressions is developed for the inductor configurations such as turns *T*, inner diameter *D*, line width *W*, and line spacing *S*. The series inductance is calculated by the physics-based closed-form expression [2]. In our model, the L_i is equaled to L_s and the *M* which is 0.15 times L_s extracted from IE3D. The other parameters R_s, C_p, C_{ox}, C_{sub}, and R_{sub} are calculated by the physics-based formulae [3]. Moreover, R_i as 0.19 times R_{sub} is extracted by modeling [1]. Figure 2 and 3 show *Q*-curve versus frequency and the frequency response of quality factor slope, respectively. The quality factor slope is defined by the rate of quality factor change. On the both side of the maximum quality factor Q_{max} we can group the slopes into two types, low frequency (LF) region with positive slopes S_L, and high frequency (HF) region with negative slopes S_H. There is a very interesting picture. The *Q*-curve is covered by a triangle composed with the LF-line, HF-line, and self resonant frequency (SRF) point. Once the circuit requirement is proposed, the slope of S_L and S_H, and SRF can be decided by the required *Q* and the corresponding frequency. The model and the inductor configuration can be exactly determined by way of design automation methodology link up the triangle.

3. Model Validation and Design Methodology

Table I summarizes the design parameters for each square, planar spiral inductors were fabricated in TSMC 0.35μm CMOS process. Figure 4 shows the measured versus simulated inductance and the number of inductors, in %, which exceeds error for our formula. Maximum error that is made using the expression [2] is less than 7%. To demonstrate the validity of our model, we have confirmed the simulated S11 and quality factor matched very well with the measured, as shown in Fig. 5 and 6, respectively. Beside the ones higher than the resonant frequency, they show good agreements between the measured and simulated S11. Among these inductors, the total error between the measured and simulated S11 below the SRF is less than 0.71%, as shown in Table I. In Fig. 6, no matter what inductances, the *Q*-curve is always confined by the triangle, composed with LF-line, HF-line, and SRF-point, as described in section 2. Table II shows the verification on characteristics of measured and simulated *Q*-curve to demonstrate the accuracy. Among these inductors, the errors of SRF and S_H are almost lower than 8.7%. Those demonstrate that the substrate loss can be predicted accurately by our model. Although the errors of S_L on large inductance ones are larger than the other characteristics, but the errors of the maximum quality factor, the most important parameter, are less than 9.2%. Regardless of inductor design on any variation of configuration or different inductances, our model shows a good validation. Figure 7 shows the number distribution of acceptable structures for the criteria of 1.5nH and *Q* exceeded 6 at 5GHz versus SRF and S_L. Obviously all of the acceptable structure is located in the lower right region. In addition, there is always a peak appeared at a SRF range for each S_L range. As the S_L diminishing, the peak will move toward higher frequency. The working point located at LF or HF region of inductor depended upon the SRF. Even the working *Q* value would promote with the higher S_L, so the SRF shall shift to lower frequency go with larger S_L to meet the requirement, then the substrate noise shall be also raising as a consequence of the working point located at HF region of inductor. The problem of substrate noise in SoC can be disregarded by extra criteria on SRF which must be larger than 3 times the working frequency. Figure 8 shows the methodology for efficient spiral inductor design automation. Our design procedure will be very attractive in future RFIC SoC applications.

4. Conclusions

We developed an efficient modeling technique to analyze spiral inductors and an optimization methodology for design automation. The accuracy of model has been proved by comparison with measurement for any configuration of inductors. We proposed a strategy, which *Q*-curve correlated to triangularity, to design the spiral inductor. The performance of the design does not only meet the circuit specification, but also rapid completion of the optimization.

Acknowledgements

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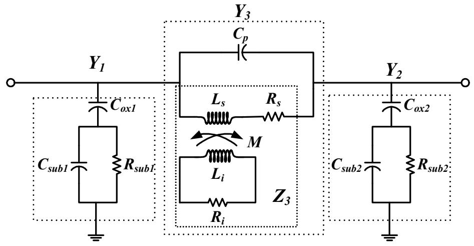

Fig. 1 A twelve-element model that involved the EM losses of a spiral inductor on lossy Si-substrate.

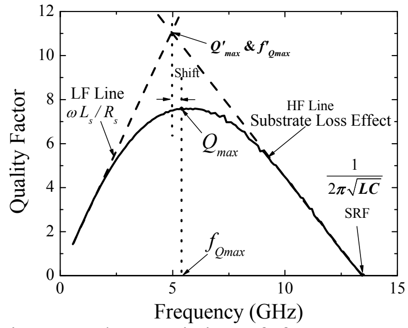

Fig. 2 Characteristics of frequency response on quality factor.

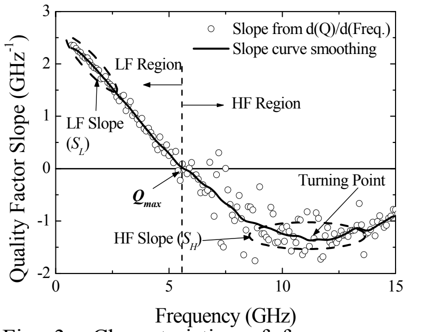

Fig. 3 Characteristics of frequency response on quality factor slope acquired by differentiating Q-curves.

Table I. The configuration of square, planar spiral inductor in 0.35μm CMOS processes.

L (nH)	Inner D. (μm)	Turns	Width (μm)	Spacing (μm)	S11 total error (%)
1.4	233	1.5	20	3	0.71
2.7	179	2.5	17	1	0.54
3.0	184	2.5	9	2	0.2
4.3	250	2.5	8	1	0.66
6.1	197	3.5	6	4	0.67

$$\text{Total error}: \ \varepsilon_{total}(S) = 100 \cdot \left\{ \sum_{freq} \left| \text{meas}S - \text{sim}S \right|^2 \Big/ \left| \text{meas}S \right|^2 \right\} \Big/ N_{freq}$$

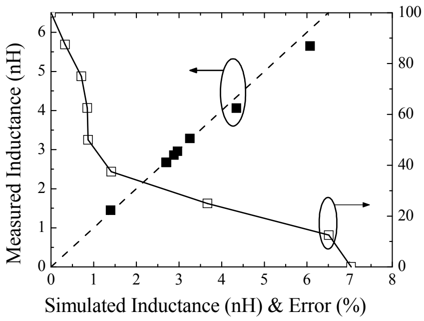

Fig. 4 Measured versus simulated inductance and the number of inductors, in %, which exceeds error for our formula.

Table II. The measured and simulated Q of square, planar spiral inductor in 0.35μm CMOS processes.

L (nH)	SRF (GHz)	Error (%)	LF Slope	Error (%)	HF Slope	Error (%)	Max. Q	Error (%)
1.4	15.7	4.9	2.46	6.9	-0.8	8.7	7.12	0.2
2.7	10	2.0	3.0	5.4	-0.99	4.5	5.97	8.5
3.0	12.4	2.4	1.90	3.6	-0.9	4.4	5.66	0.6
4.3	8.7	0	1.91	16.1	-1.08	7.6	4.4	9.2
6.1	8.3	1.2	1.69	14.2	-0.98	3.5	3.71	8.1

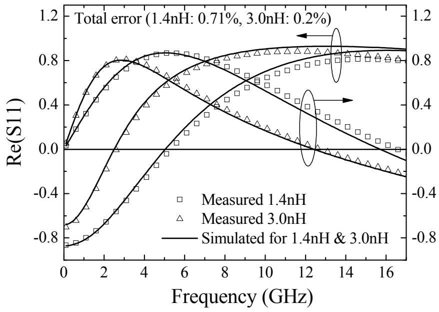

Fig. 5 Measured S11 and simulated of 1.4 and 3.0 nH of the 0.35μm square, planar inductors.

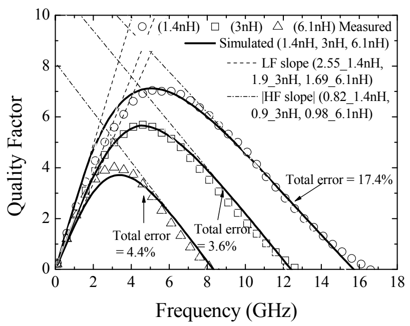

Fig. 6 Measured Q value and simulated of 1.4, 3.0, and 6.1 nH of the 0.35 μm square, planar inductors.

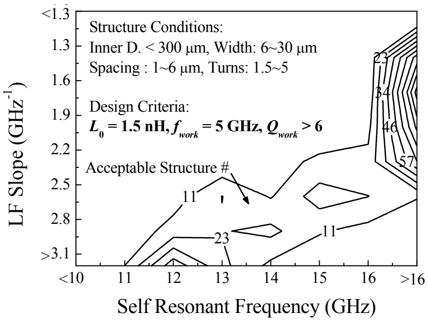

Fig. 7 The number distribution of acceptable structures for the criteria of 1.5nH and Q exceeded 6 at 5GHz versus SRF and S_L.

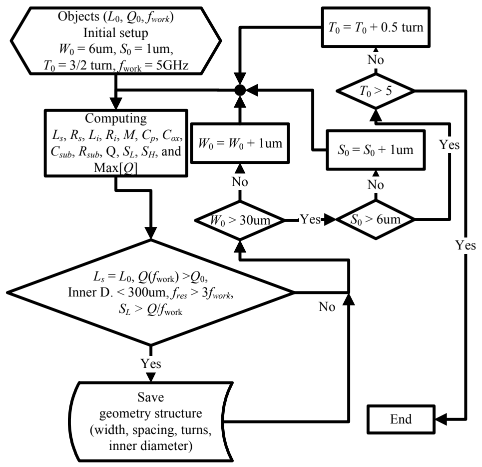

Fig. 8 The methodology for efficient spiral inductor design automation.