C-7-4

Enhanced Power Supply Structure with New Mesh Wiring and Electroless Plated Shunt Line and Assembly-Stress-Relaxation Structure

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Introduction

Recently an increase of power consumption caused by miniaturizing LSI with scaling down become a serious issue and suppressing the increase of IR drop within a chip is necessary for high speed operation. In addition, since more fragile low-k materials are applied to interlayer dielectric films, it becomes a key issue to relax stresses in assembly processes, e.g. probing, wire bonding and plastic molding. Therefore the structure of global layers is essentially important. Against the above mentioned problems, adding global layers is conventionally adopted[1], however chip cost is up.

In this paper, we have developed new structures without adding global interconnect layers:

1) New mesh wiring structure
2) Electroless plated shunt line structure
3) Assembly-stress-relaxation structure

These structures are expected to reduce IR drop and to relax assembly stress.

New mesh wiring structure

Due to the increase of power consumption, many thick global interconnects are currently applied to the power supply lines. In general, thicker global interconnects are used on the upper layer as shown in Fig.1. Conventional mesh wiring of power supply is illustrated in Fig.2. Each layer of power supply wiring is perpendicular and same potential wirings are connected with vias. Since each layer is perpendicularly arrayed with different thickness, there appears different resistance depending on the direction as whole global layers. Resultantly IR drop distributed. And then this often leads to big IR drop at the center of the chip with power supply in the vicinity of the chip corner, as shown in Fig. 3. We have developed a new mesh wiring structure as illustrated in Fig.4 to reduce maximum IR drop at the center of the chip. In the new mesh wiring structure, adequately fixed size blocks of mesh wiring structures are arrayed and each block is alternately rotated to eliminate directional dependence of resistance. As shown in Fig.5, the directional dependence of IR drop disappeared since this structure can supply the averaged resistance in a whole chip area. We have succeeded in reducing IR drop by 20% as shown in Fig.6.

Electroless plated shunt line structure

We have developed another method of decreasing IR drop by reducing resistance of global interconnects. To present low-cost method compared to that of adding or thickening a global layer, we have applied electroless plated shunt line structure to the global layer. By means of Ni electroless plating which is widely used as UBM (under bump/ball metal), it is possible to obtain the plated shunt line during the formation process of UBM on bonding pads. We have removed passivation films not only on bonding pads but also on power supply lines (Cu, 1.5μm thickness) and then made Ni electroless plating (5μm or 10μm thickness) both on bonding pads and power supply lines. Fig.7 is an SEM image of Ni electroless plated power supply lines. We have examined 3 different types of Ni electroless plating (Ni-P 7wt%, Ni-P 1wt%, Ni-B) and, the results of change in wiring resistance are shown in Fig.8. We have successfully obtained reduction in resistance by 38% with 10μm-thick Ni-B electroless plated shunt line structure.

Assembly-Stress-Relaxation Structure

As low-k films are becoming more fragile with scaling down of technology node. This makes it important to reduce assembly stress on low-k films.

We have shown the effect of assembly stress onto the transistor's current, using transistor array as shown in Fig. 9,10. As the change in drain current is in proportion to the stress applied to transistors, it is possible to evaluate relative stress applied to the area beneath global layer by comparing the peak value of Δ Ids[2][3].

We have demonstrated the effect of assembly-stress-relaxation structure with Ni plating, on relaxing assembly-stress. In Fig.11, we show the result of the change in drain current under probe-induced stress, regarding 4 different structures. We have found the effect on reducing assembly stress to 77%, 27%, and 7% (2 global, 1 global + 5μm Ni, 1 global + 10μm Ni). Therefore, Ni electroless plating is seemed to be more effective than adding 1 global layer and resultantly we have succeeded in reducing assembly stress to 7%.

Conclusions

We have successfully developed the new mesh wiring structure with no directional dependence of wiring resistance and electroless plated shunt line structure to decrease IR drop. We have succeeded in reducing IR drop by 20% with the new mesh wiring structure, and resistance by 38% with electroless plated shunt line structure. Furthermore, as the plated structure is simultaneously formed with assembly-stress-relaxation structure, the increase of chip cost does not appear surely.

We have also found the effect of the assembly-stress-relaxation structure with plating. This structure can dramatically reduce assembly stress, resultantly ΔIds has been obtained to be 7% compared to that of conventional structure.

References

[1] ITRS 2005 Interconnect p.8.
[2] K.Harafuji, et al., Jpn. J. Appl. Phys. **47** (2008) 824.
[3] K.Takemura, et al., SSDM (2006), paper D-6-3.

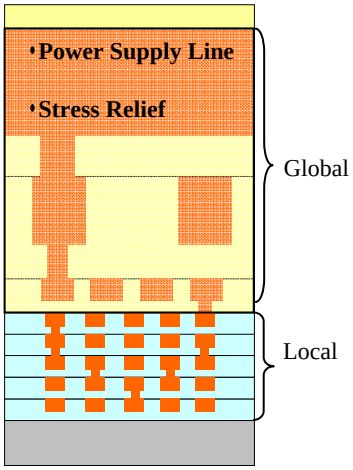

Fig.1 Cross Section of LSI.

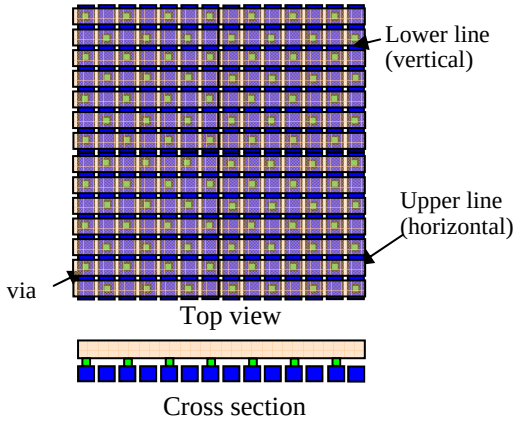

Fig.2 Conventional mesh structure.

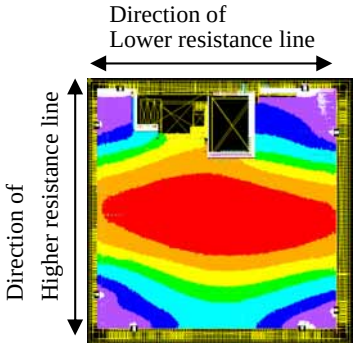

Fig.3 IR drop map in conventional structure.

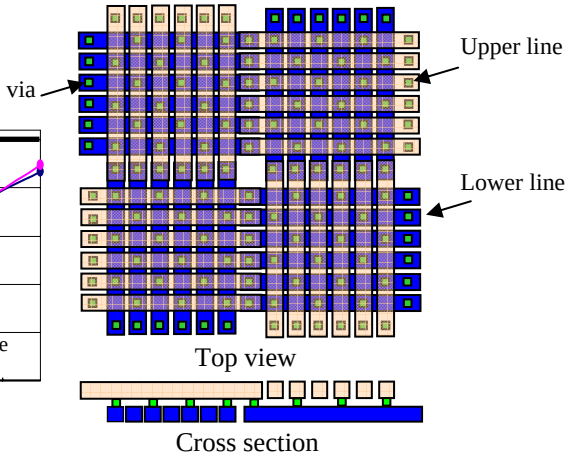

Fig.4 New mesh structure.

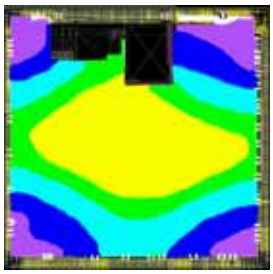

Fig.5 IR drop map in new structure.

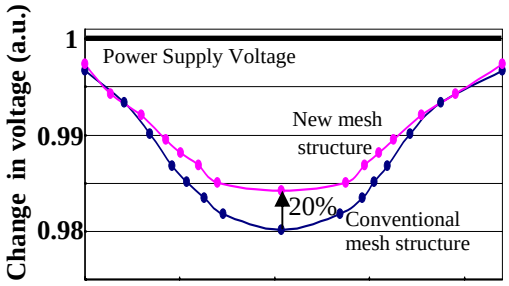

Fig.6 Cross Section of Potential map.

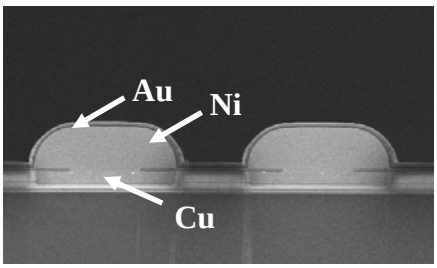

Fig.7 Cross section of plated shunt line.

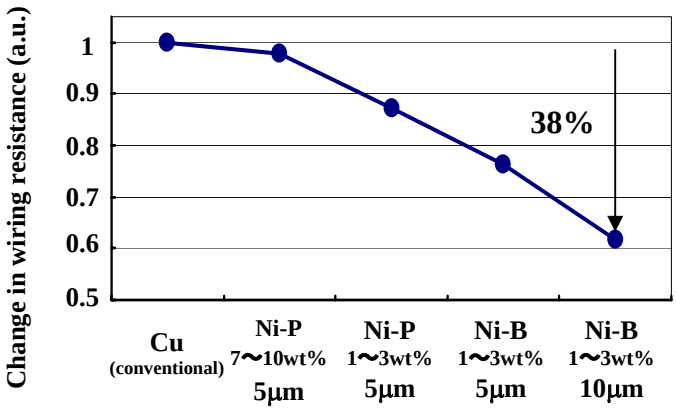

Fig.8 Comparison of plated shunt line resistance.

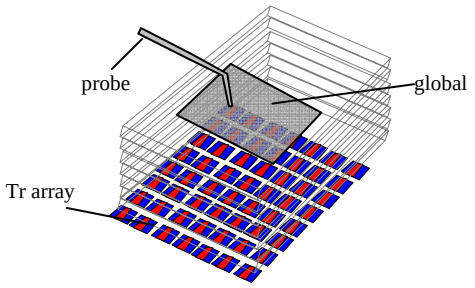

Fig.9 Schematic illustration of transistor array structure.

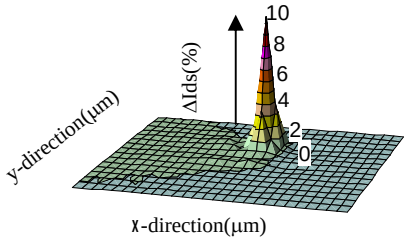

Fig.10 Transistor characteristic change under probe induced stress.

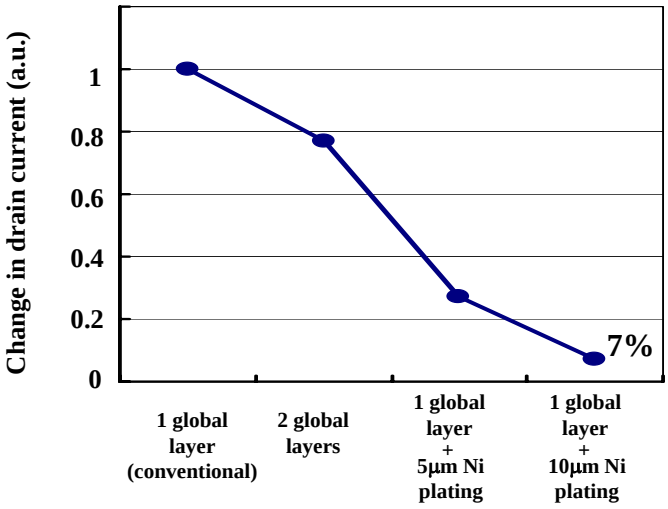

Fig.11 Relaxation effect of assembly stress.