Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 910-911

C-8-4 (Invited)

# Interconnect and packaging technology for CMOS image sensors

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## 1. Introduction:

CMOS image sensors are increasingly being used in consumer products instead of charge-coupled devices, because of lower power consumption, lower system cost, and the ability to randomly access image data [1]. Image sensors require a number of unique processes for on-chip interconnects and for packaging. In this paper, we give an overview of these processes.

## 2. Basis Operation

The CMOS imager consists of an array of pixels that detect the incident light. A commonly used pixel is the four transistor or "4T" cell (Fig. 1) [2]. To capture an image, the photodiode is first reversed biased (set to Vdd) using the reset gate and transfer gate (Fig. 2). When the shutter of the camera is opened, light that is incident on the photodiode will generate electron-hole pairs. To sense the charge in the photodiode, the transfer gate is turned on and the charge is moved to the floating diffusion. This changes the potential on the gate of the the source-follower circuit, and the resulting signal is detected at the output of the pixel by turning on the row select transistor.

The photo-diode area is much smaller than the total area of the pixel. To overcome this loss of sensitivity, microlenses are used to focus light on the photo-diodes [3]. The quantum efficiency (i.e., the percentage of photo-generated carriers that are detected for each incoming photon) is greatly improved by using microlenses . In order to capture color information from the broad bandwidth incident light, color filters are used so that each pixel captures mainly one color of light (i.e., red, green, or blue). The color filters consist of dyed photoresist that is arranged in alternating rows or either green and blue or green and red [4]..

## 2. Interconnect Process

For small pixel sizes (< 3 μm), the optical stack height critically determines the angle response of the detector, which is especially important at the edge of the array (Fig. 6). By using Cu instead of Al [5], the stack height can be reduced improving the angle response. However, the SiN capping layers used to passivate the surface of the Cu introduce discontinuities in the refractive index, that can reflect light and reduce the sensitivity of imager [5]. By removing the SiN capping layer in the optical path (Fig. 3), the full benefits of the reduced stack height can be achieved.

As pixel size is reduced below 2 μm, better sensitivity is required. One method to improve sensitivity is to use a lightpipe process, to guide line down to the photodiode [6,7]. The lightpipe process requires an additional etch to remove the dielectrics over the photodiode and a fill step (Fig. 4). A fill material is required that has a high refractive index, in order to achieve total internal reflection when light enters at a high incidence angle.

Another option for improving the image sensor sensitivity at small pixel sizes is to use backside illumination [8-10]. Backside illumination eliminates the light blocking problems associated with the metallization, resulting in improved quantum efficiency. After conventional processing, the frontside of the wafer is attached to glass wafer for mechnical support, then thinned to 5 to 10 μm [8-10]. Using backside illumination, the sensitivity of the imager can be increased by almost 40% [9].

## 3. Testing and Packaging

Image sensor testing requires special equipment, for measuring the optical properties of the device, as well as the electrical properties [11,12]. It should also be noted that imager sensors are sensitive to defects that would not affect a standard integrated circuit. For example, large particles (i.e. on the order of the pixel size) that fall on the imager array during test, shipping, backgrinding, or dicing, can impact yield, because they block light from the photodiode [13]. .

There are a number of different packaging options for image sensors. The cheapest process is "chip-on-board", where the image sensor is diced, then directly mounted on the printed circuit board [14,15]. The main disadvantage of this approach is yield loss associated with particles falling on the imager array during the packaging process.

To eliminate the yield loss associated with packaging, a number of wafer-scale packaging methods have been applied to image sensors [16,17]. For the wafer-scale package, the first step is to cover the wafer with a glass plate, using a spacer to form an air cavity between the microlenses on the wafer and the the glass (Fig. 5). The glass plate protects the microlenses from particles associated with packaging, thereby improving yield. To access the bond pads, additional steps are required. These consist of

backside wafer thinning, via formation, dielectric deposition (to isolate the via from the substrate). The first wafer-scale packages for image sensors [16] used edge connections to the bond pads. More recently [17], through-silicon-vias are used to access the bond pads (Fig. 5).

Image sensors for cell phone cameras are often fabricated using a package-on-package process [18], with the image sensor array on top layer and the digital circuits for image processing on the lower layer. This approach provides a smaller form factor, but has a relatively interconnect density between the two chips. More advanced 3D stacking with through-silicon-vias is being investigated [19], which provides high interconnect density between the different layers. A larger number of transistors can be used per pixel while still achieving a high fill factor for the photodiodes to provide . The additional transistors in the pixel can be used to improve performance, providing high dynamic range [20], high speed and high sensitivity [21].


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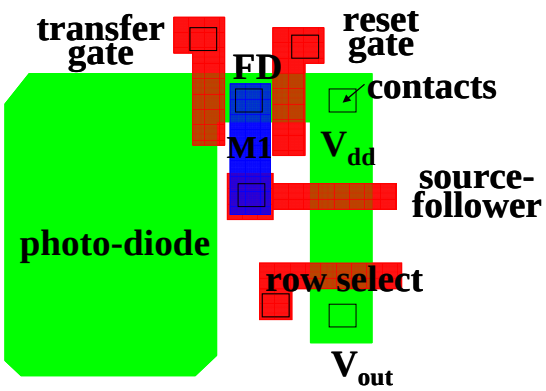


Fig. 1. Layout of 4T pixel for CMOS image sensor.

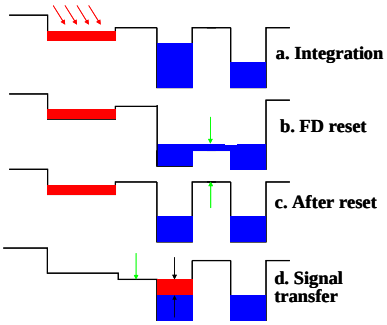


Fig. 2. CMOS image sensor operation.

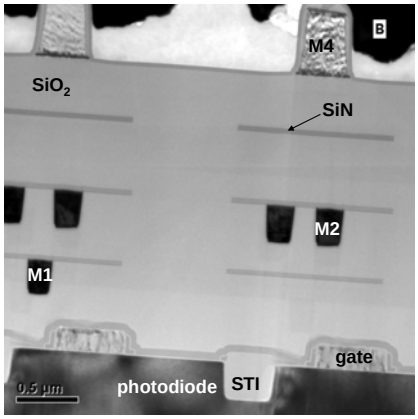


Fig. 3. TEM of CMOS image sensor with Cu wires.

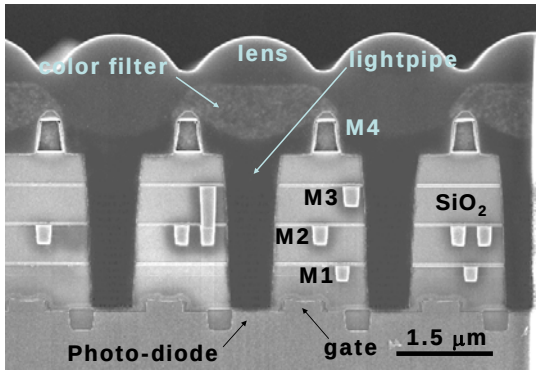


Fig. 4. SEM of CMOS image sensor with lightpipe.

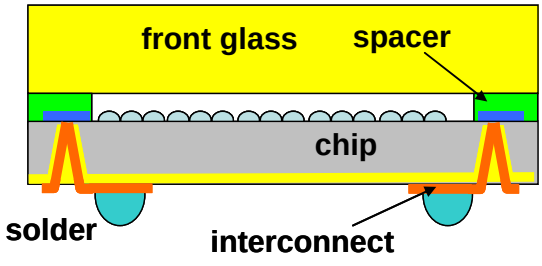


Fig. 5. Wafer-scale package for image sensor (ref. 17).