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Metal resistivity in narrow interconnect lines

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1. Introduction

In order to achieve high performance in advanced nodes, interconnect technology requires low resistance and highly reliable wires. To obtain these characteristics, Cu damascene technology succeeded to Al technology in the late 90's thanks to the lower resistivity of pure bulk Cu (1.67 vs 2.65 μΩ.cm) and to it superior resistance to electromigration. However, as far back as 1998, a first paper presented experimental results on a so-called "size effect" [1]: when Cu line dimensions are reduced, a large increase of Cu resistivity is observed. It is illustrated in Fig. 1. Numerous following publications confirm this result. Since 2001, this behavior has been integrated in the International Technology Roadmap for Semiconductor (ITRS) as one of the top 10 challenges of interconnect technology [2]. To mitigate the size effect, two main approaches have been conducted: decrease of metallic barrier thickness using advanced barrier processes or direct work on the origin of size effect. This approach is discussed in this paper. First, the physical origin of size effect is presented. The impact of the damascene technological options on Cu resistivity is discussed. Finally, recent results on a possible way to optimize resistivity with respect to industrial constraints are presented.

2. Physical origin of size effect.

The conductivity of a metal is directly proportional to the mean free path of the electrons. At 303K, the latter is equal to 38nm in Cu to be compared to typical line width and grain size which are smaller than 100nm. Furthermore, grain size is proportional to line width [3-5]. As a consequence, electron scattering increases both at barrier-Cu interface and at grain boundaries (cf. Fig. 1). Thus, as experimentally observed for thin films at the beginning of the 20th century [6], a large metal resistivity increase occurs. Our recent experiments demonstrate the correlation between grain size and resistivity for narrow Cu interconnects [7].

General models of resistivity in narrow line have been proposed following Fuchs–Sondheimer [8, 9] and Mayadas-Shatzkes [10] pioneer works [11, 4]. The main adjustable parameters are p, the probability of elastic reflection of the electrons at the surface, R, the occurrence of charge carriers' diffusion when they intercept grain boundaries and ρ_0 the bulk material resistivity which includes contamination effects. A precise determination of these parameters is required for classification of major effects. To do so, dedicated experiments are required. They can be based either on full temperature range resistivity measurement [12, 13], on precise thin film experiments [14] or on extensive geometrical parameter variations [5]. In the case of Cu narrow lines confined with Ta, an illustration of the different contributions to resistivity is reported in Fig. 1. Results suggest high surface effect, medium grain boundary effect and low impurity content inside the lines.

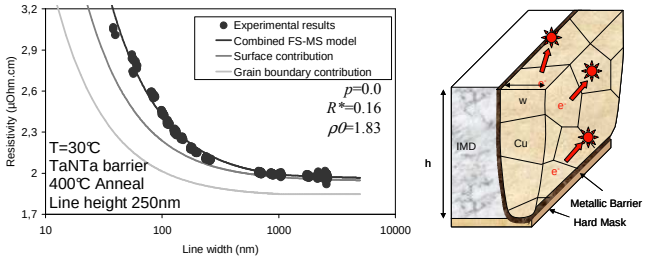

Fig. 1: Resistivity vs line width for Cu lines [5]. A schematic view of electron reflection in narrow Cu line is also reported.

3. Process integration impact

Surface

Due to the previously described large impact of Cu barrier surface on resistivity, one may expect that engineering of barrier material could reduce electron scattering. Unfortunately, to our knowledge, the used of different barrier layers (Ru, WN, ALD TaN, TiN, TiSiN) show no improvement on Cu resistivity [15-17].

Impurity

Electro-Chemical Deposition method (ECD) is used to achieve narrow lines superfill with Cu. This process requires additives which lead to the incorporation of impurities in the deposited film. Used of advanced ECD electrolyte can reduce contamination as shown on SIMS analysis presented in Fig. 2 [18]. For narrow lines, a slight decrease in Cu resistivity is observed with respect to the reference electrolyte (cf. Fig. 3).

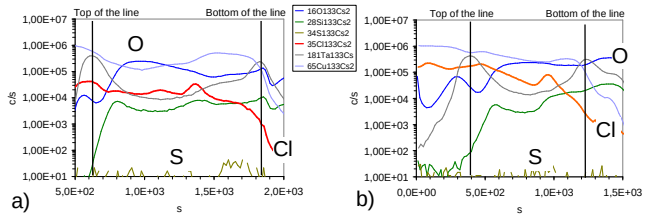

Fig. 2: SIMS analysis of 90/90nm patterned structure after 400°C anneal. a) new generation electrolyte, b) reference electrolyte [18]

The resistivity model and the grain size observations suggest that this decrease is mainly due to grain boundary effect: it seems to be the signature of higher grain size resulting from grain boundary mobility enhancement. From a technological point of view, new generation electrolytes appear to be a usable parameter to counteract the size effect in interconnects.

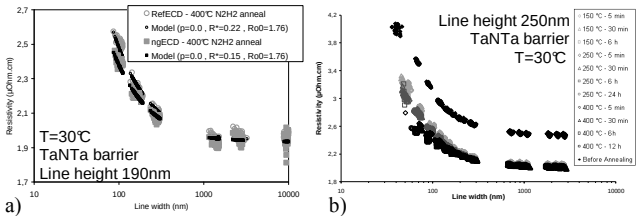

Fig. 3: Resistivity vs line width. a) Impact of Cu ECD chemistry. [18] b) Impact of furnace anneal. [7]

4. Reducing size effect by grain size optimization

In the standard process flow of Cu lines, an annealing is performed after Cu ECD, when the Cu surplus is still present. The grain growth occurring during anneal greatly reduces the Cu resistivity (cf. Fig. 3 b)). Applying high thermal budget, a relatively low Cu resistivity is achieved.

In-line grain microstructure results from a kinetic competition between grain growth inside the line and invasion by grains originated from the overburden as illustrated in Fig. 4. For large lines, total extension of overburden grains in damascene trenches is observed (c). Large grains and a bamboo structure perpendicular to the substrate are then obtained (f). When line width is reduced, the behaviour depends on line height and annealing conditions (cf. Fig. 5): at temperature above 400°C total overburden grain extension occurs whereas at lower temperature partial overburden grain extension is observed. The microstructure is then controlled by growth mechanisms inside the pattern; grain morphology is equiaxial and grain size closed to the line width (cf. Fig. 4 e)).

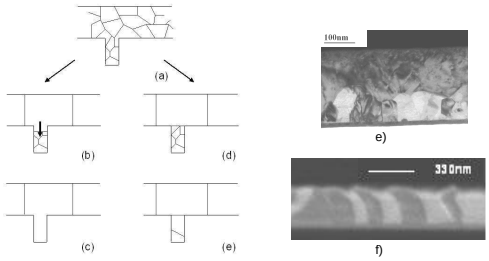

Fig. 4: Schematic view of grain growth mechanisms in damascene architecture. (e) and (f) are longitudinal view of Cu lines after a 150°C 5mn anneal with respectively 70nm and 150nm line width.

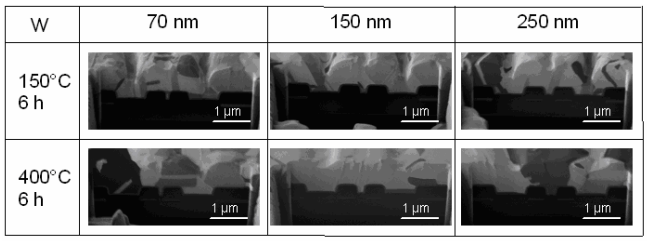

Fig. 5: Cross-section view of Cu line before CMP. Variation of line width and annealing conditions. The structure is composed as follow: a single narrow line of a given width surrounded by two 600 nm width line. [19].

Overburden grain extension can be quantified using a method based on Cu line resistivity when annealing is performed either before or after CMP [19]. Fig. 6 reports the decrease of the copper overburden microstructure depth of invasion inside the trench when line width decreases. For a given annealing condition, this plot gives the trench depth that maximizes overburden grain effect in trenches for a particular line width. Using these results, for a low thermal budget, line height during Cu filling can be optimized regarding Cu microstructure and resistivity.

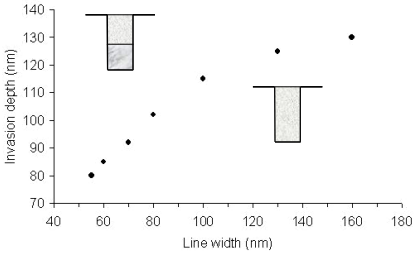

Fig. 6: Cu overburden microstructure invasion depth vs line width for copper lines annealed at 150°C during 6 hours. [19]

5. Conclusions

Counteract Cu size effect is one of the key point of the scaling of interconnects. In it 2001 edition, ITRS states that "Cu interfaces, microstructures and impurity levels will be engineered to alleviate the impact of this resistivity rise for a few additional technology generations".

To our knowledge, no solution using interface engineering have been proved. Suggestions to optimized Cu microstructure and resistivity are presented in this paper based on impurity and microstructure engineering. They require either simple modification of Cu process or optimization of the integration scheme.

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