Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 70-71

D-1-1 (Invited)

Millimeter-Wave CMOS Pulse Communication

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1. Introduction

Recently, the well-known feature of millimeter-wave communication has attracted attention because millimeter-wave circuits have been realized with advanced CMOS technologies. In academic conferences and journals, many studies on millimeter-wave CMOS circuits were reported in the past few years, and consumer devices are expected to be available soon.

Here, for realizing the consumer application of millimeter waves, the reduction of power consumption is the most important issue. It is noted that the power-hungry building blocks in a transceiver shown in Fig. 1(a) are the local oscillator (LO) based on the phase-locked loop (PLL). If these blocks can be eliminated in a transceiver, power consumption will be considerably reduced. From this viewpoint, we have studied millimeter-wave pulse communication shown in Fig. 1(b) for high-performance CMOS wireless transceivers. In this paper, low-power pulse generator and receiver, which are the most important building blocks in millimeter-wave pulse communication, are discussed for high-speed wireless communications using the 60 GHz band.

2. 60GHz CMOS Pulse Generator [1]

A 60GHz CMOS pulse generator comprises multiple monopulse generators. The monopulse generator consists of a delay cell and an edge combiner, as shown in Fig. 2, where the former is composed of two CMOS inverters and the latter is composed of two nMOSFETs. Two transistors of the edge combiner generate a single monopulse by applying an AND operation. After consecutive monopulses are generated, they are again combined by a wired OR to generate a spectrum-limited pulse. Figure 3 shows a chip micrograph of the CMOS pulse generator with a die area of $590\times380\mu m^2$, where a 90nm CMOS process with nine metal layers was used. To The time-domain response of the pulse generator is shown in Fig.4, where the 62.5GHz operating frequency is observed at a supply voltage of 1.15V. Figure 5 shows carrier frequencies and output powers as function of supply voltage, and also shows power consumptions as function of input data rate. The carrier frequency increased with supply voltage with inverse proportional relationship, while output power is almost unchanged when supply voltage is higher than 0.7V. The linear dependence of power consumption on input data rate is confirmed by the measurement data. Since power is only consumed at rising edges of the input signal, the power consumption for the proposed pulse generator is 11.5mW at a supplies voltage of 1.15V.

3. 60GHz CMOS Pulse Receiver [2]

Over-Gbps communication will have low power consumption when a received signal is detected without using a high-frequency LO and high-speed data are processed using only a limiting amplifier (LA), as shown in Fig. 6(a). A 60GHz-band CMOS pulse receiver used for investigating the above concept is shown in Fig. 6(b). The receiver was fabricated by a 90nm CMOS process. A micrograph of the receiver is shown in Fig. 7. The eye diagram and bit-error rate (BER) of the receiver are obtained using 2^{31}-1 bits of pseudo-random data. The eye diagram of the receiver is shown in Fig. 8 for the data rates of 1 and 2Gbps. In both cases, clear eye openings are observed. The output was 313mV peak to peak. The measured BER with respect to the average pulse power is plotted in Fig. 9 for 1 and 2Gbps data rates. The total power consumption of the pulse receiver including the buffer is 19.2mW. To compare between this receiver and optical receivers, a figure of merit FOM is determined as $G{\cdot}DR/P_{DC}$, where G is the power gain, DR is the data rate, and P_{DC} is the power consumption. The product of G and DR is plotted as a function of P_{DC}, as shown in Fig. 8, where the FOMs are given by the slope. The FOM of this receiver is a slightly better than those of other reported optical receivers.

4. Conclusions

In this paper, 60GHz pulse generator and receiver for realizing low-power and high-speed communications were described. By designing pulse generator and receiver, a millimeter-wave pulse can be generated and detected without using a power-hungry LO. As a result, the pulse circuits consumes a small amount of power. The study of CMOS millimeter-wave pulse communication will encourage the widespread adoption of consumer millimeter-wave applications.

Acknowledgements

This study was partially supported by the core research for evolutional science and technology (CREST) of the Japan Science and Technology Agency. The chip was fabricated by the chip fabrication program of the VLSI Design and Education Center (VDEC), the University of Tokyo, in collaboration with STARC, Fujitsu, Ltd., Matsushita Electric Industrial Company, Ltd., NEC Electronics Corporation, Renesas Technology Corporation and Toshiba Corporation.

References

[1] Wasanthamala, et al., Elec. Lett., pp. 100-102, 2007
[2] Oncu, et al., VLSI Circuits, 2008
[3] Narasimha, et al., ISSCC, pp. 42-43, 2007.
[4] Le, et al., ISSCC, pp. 474-540, 2004.
[5] Sankaran, et al., IEEE EDL, pp. 492-494, 2005.
[6] Yeh, et al., MTT-S, pp. 53-56, 2005.
[7] Palermo, et al., ISSCC, pp. 44-45, 2007.
[8] Swoboda and Zimmermann, ISSCC, pp. 904-911, 2006.
[9] Chen and Gan, VLSI Circuits, pp. 120-121, 2006.
[10] Krishnapura, et al., ISSCC, pp. 60-61, 2005.
[11] Werker, et al., ISSCC, pp. 172-173, 2004.

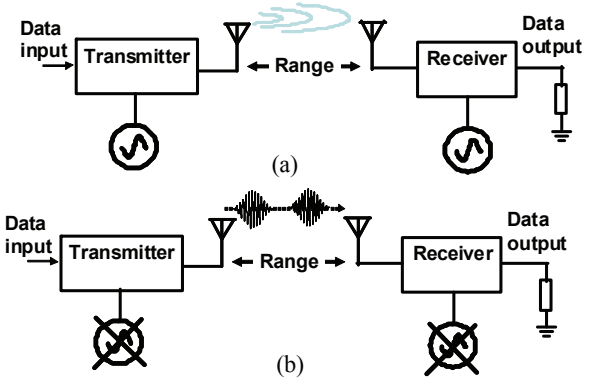


Fig. 1. Schematic building blocks for wireless communication based on (a) carrier modulation and (b) pulse modulation.

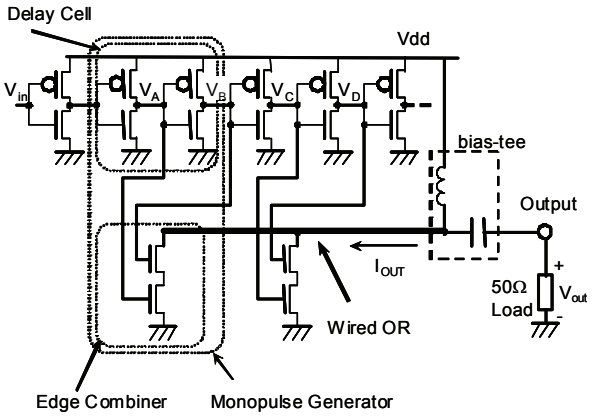
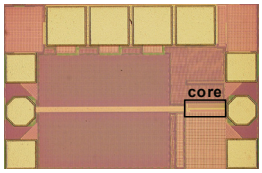


Fig. 2. Circuit topology of a 60GHz CMOS pulse generator.



Chip micrograph CMOS 90nm (nine metals one ploy)

Technology	90nm CMOS
Frequency Band	59-66GHz
Modulation	PPK
Supply Voltage	1.15V
Input Data Rate	1.5Gbps
Power Consumption	11mW@ 1.5Gbps
Core Size	90μm × 20μm

Fig. 3. Chip micrograph and specification of 60GHz CMOS pulse generator.

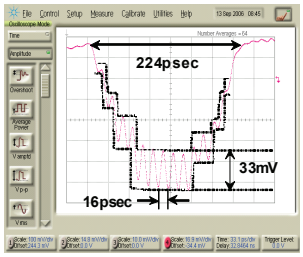


Fig. 4. Measured transient response of 60GHz CMOS pulse generator.

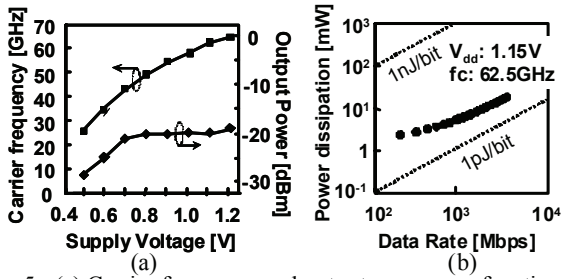


Fig. 5. (a) Carrier frequency and output power as a function of supply voltage and (b) power dissipation as a function of input data rate.

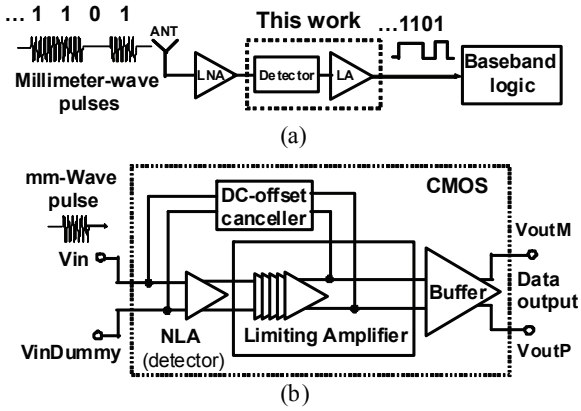


Fig. 6. (a) Receiver building block for millimeter-wave pulse communication and (b) CMOS pulse receiver.

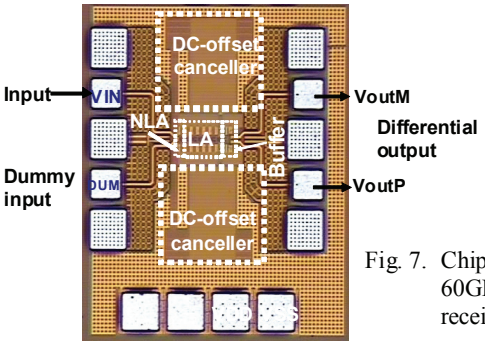
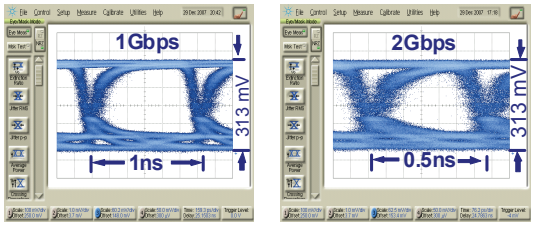


Fig. 7. Chip micrograph of 60GHz CMOS pulse receiver.



(a) (b)

Fig. 8. Eye diagram at the output of CMOS pulse receiver in the cases of (a) 1Gbps and (b) 2Gbps.

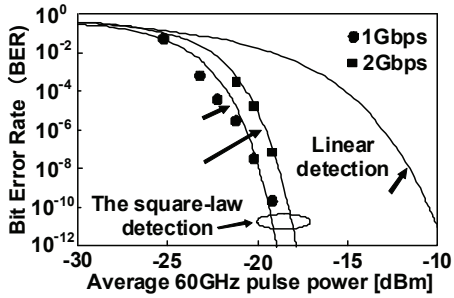


Fig. 9. Bit error rates as a function of the input power.

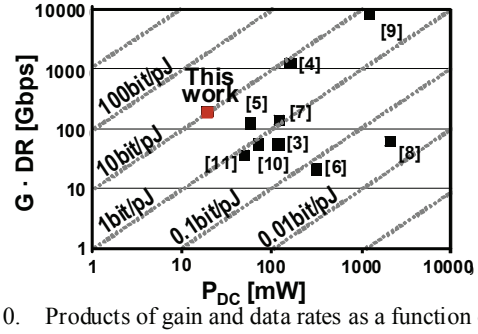


Fig. 10. Products of gain and data rates as a function of power consumption.