Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 74-75

D-1-3

A 2-GHz-band CMOS Low Noise Amplifier with High-Q Inductors Embedded in Wafer-Level Package

[1]Susumu Sadoshima, [1]Satoshi Fukuda, [2]Hiroyuki Ito, [3]Kazuhisa Itoi, [3]Masakazu Sato,
[3]Tatsuya Ito, [4]Ryozo Yamauchi, [1]Kenichi Okada, [1]Noboru Ishihara, and [1]Kazuya Masu
[1]Integrated Research Institute, Tokyo Institute of Technology
[2]Precision and Intelligence Laboratory, Tokyo Institute of Technology
4259-R2-17 Nagatsuta, Midori-ku, Yokohama, 226-8503 Japan.
Tel: +81-45-924-5031, Fax: +81-45-924-5166, E-mail: paper@lsi.pi.titech.ac.jp
[3]Electron Device Laboratory, Fujikura Ltd. 1440 Mutsuzaki, Sakura, Chiba 285-8550, Japan
[4]Fujikura Ltd., 1-5-1 Kiba, Koto-ku, Tokyo 135-8512, Japan

I. INTRODUCTION

Recent Si CMOS technologies have been achieving high f_T and high f_{max} enough to realize RF circuits. Large portions of RF functionalities have been integrated into CMOS chip. However, some discrete elements still remain on boards. One of these is an inductor used in low noise amplifiers (LNAs). On-chip inductors are widely used in modern RF CMOS circuits however they degrade noise figure (NF) of LNAs. Because on-chip inductors have low quality factor (around 10 at the highest), and resistance of input inductor becomes thermal-noise sources.

One of solutions for achieving high-Q inductors on a Si substrate is the use of wafer level package (WLP) process [1]. It has been reported that inductors embedded in WLP process (WLP inductors) have Q-factor of over 20 on the lossy Si substrate. We have simulated performances of a LNA with WLP inductors and discussed merits of WLP inductors.

The present paper fabricates and measures the LNA with WLP inductors, and we will show that NF of LNAs can be improved by applying WLP inductors. Section II reviews advantages of WLP inductors and a LNA design. In the Section III, measured characteristics of LNAs are discussed. The paper is concluded in Section IV.

II. WLP INDUCTORS AND LNA DESIGN

Two factors, resistance and substrate losses, degrade Q of on-chip inductors. Metal layers in Si LSI are thin, and on-chip wirings have large resistance. Magnetic flux induced by the inductor penetrates the lossy Si substrate; eddy current is generated in the substrate and degrades Q of inductors.

Figure 1 shows a cross section of the WLP process. This technology provides (1) low-resistive copper lines due to thick metal-layers, and (2) low substrate-loss due to thick dielectric (resin) layers that separate lines from the Si substrate and reduce induced eddy currents in the Si substrate. Thus, WLP process can improve Q of inductors. Figure 2 shows simulated Q-factors of on-chip and WLP inductors. These inductors are designed to have the same inductance 0.8 nH at 2 GHz. The maximum Q of the WLP inductor is 35 which is about 3 times higher than that of the on-chip inductor.

Figure 3 shows a schematic of the LNA for discussing impacts of WLP inductors. All inductors in the circuit are fabricated by using WLP process. The topology proposed in [3] is applied for achieving wider gain-bandwidth. The cascode topology improves a gain and a reverse isolation. The load is designed to improve the gain around 2 GHz. The value of L_{load} is set to 6.6 nH, and that of R_{load} is 50 Ω. A source-follower buffer is adopted for 50 Ω output matching.

To discuss the advantage of WLP inductors, we also design the LNA with only on-chip inductors and the same topology in Fig. 3 . For fair comparison, both LNAs with WLP and on-chip inductors have the same inductance, capacitance, transistor sizes, supply voltages and bias voltages. Only WLP inductors are substituted by on-chip inductors in the conventional LNA.

III. MEASUREMENTS AND DISCUSSIONS

0.18 μm CMOS process with RF options is used, and WLP inductors are fabricated by using our WLP process. Figure 4 shows a chip micrograph of the LNA with WLP inductors. A chip area is 2.1 mm × 1.9 mm.

Figure 5 (a) shows measured NFs of the LNA with WLP inductors (WLP LNA) and the one with on-chip inductors (on-chip LNA). Significance is that the minimum NF of LNAs can be improved by only substituting on-chip inductors with WLP inductors. Figure 5 (b) is measured S_{21} (forward transmission coefficient), and the maximum gain is 23.7 dB and 21.5 dB for the WLP and on-chip LNAs, respectively. Figure 6 shows input and output reflection coefficients. At the frequency of 2 GHz, S_{11} is -4.0 dB for the WLP LNA, and is -7.0 dB for the on-chip LNA. S_{22} are almost the same as shown in Fig. 6, because the same output buffer circuit is used in both LNAs. Performances of two LNAs are summarized in Table I.

IV. CONCLUSION

The LNA with high-Q inductors embedded in WLP process was presented and was compared to the conventional one with only on-chip inductors. Measurement results showed that NF of LNA can be improved by replacing on-chip inductors with WLP inductors. WLP inductors are expected to improve noise characteristics of modern RF circuits because they depend on Q of inductors. The introduction of WLP inductors would provide big benefits to RF circuits especially in future CMOS processes that have thinner metal and dielectric layers.

Acknowledgement

This work was partially supported by NEDO, MEXT. KAKENHI, JSPS. KAKENHI, MIC. SCOPE, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd.

References

[1] K. Itoi, *et al.*, "On-Chip High-Q Cu Inductors Embedded In Wafer-Level Chip-Scale Package for Silicon RF Application," *IEEE MTT-S Int. Microwave Symp.*, pp. 197-200, June 2004.

[2] S. Fukuda, *et al.*, "A 5.2GHz CMOS Low Noise Amplifier with High-Q Inductors Embedded in Wafer-Level Chip-Scale Package," *International Workshop on RF Integration Technology*, pp. 34-37, 2007.

[3] A. Bevilacqua and A. M. Niknejad, "An ultra-wideband CMOS LNA for3.1 to 10.6GHz wireless receivers," in IEEE ISSCC Dig. Tech. Papers, San Francisco, California, Feb. 2004, pp. 382.383.

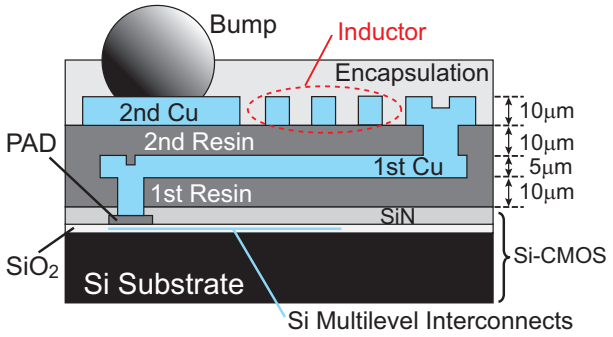


Fig. 1. Cross section of WLP.

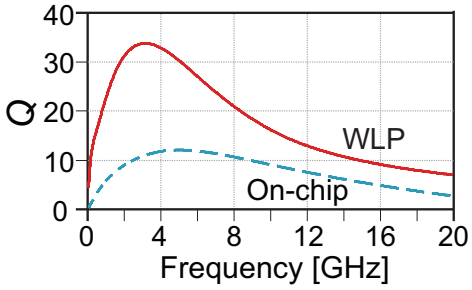


Fig. 2. Simulated quality factors of WLP and on-chip inductors.

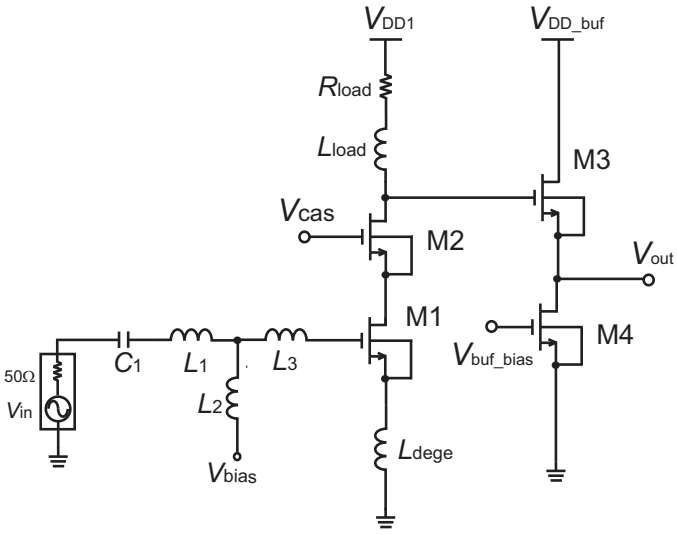


Fig. 3. Schematic of the LNA.

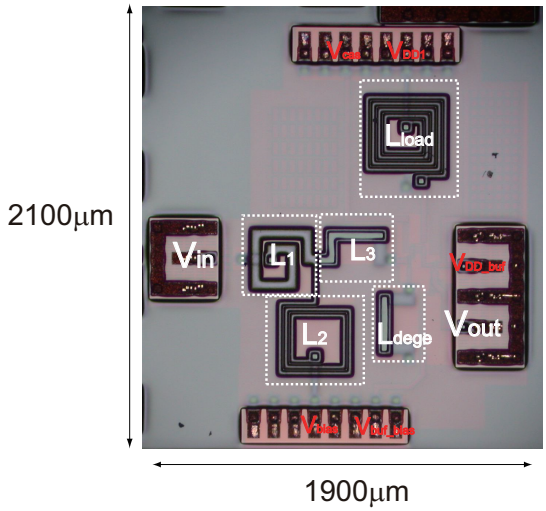
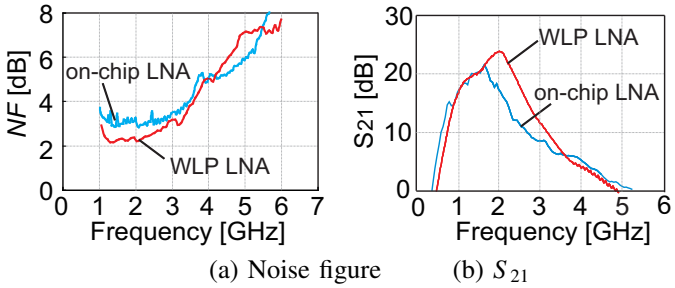
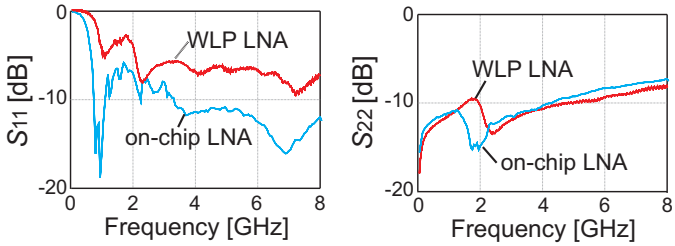


Fig. 4. Chip micrograph of the LNA with WLP inductors (WLP LNA).



(a) Noise figure (b) S_{21}

Fig. 5. Measured noise figure and gain.



(a) S_{11} (b) S_{22}

Fig. 6. Measured input and output impedance matching.

TABLE I

PERFORMANCE SUMMARY.

	WLP LNA	on-chip LNA
Tech.	0.18 μm CMOS+WLP	0.18 μm CMOS
Power supply [V]	1.8	1.8
Frequency* [GHz]	2.0	1.65
Maximum Gain [dB]	23.7	21.5
NF [dB]	2.2	3.1
Power consumption [mW]	14	14

*S_{21} (gain) becomes maximum at this frequency.