A High IIP3 Image Rejection Filter with Current Adapted Buffers for a Digital/Analog TV Tuner IC in a 0.25µm RF-CMOS Technology

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1. Introduction
A single chip TV tuner IC is becoming popular rather than a conventional can-type tuner module with discrete components and even outperformed by a recent state-of-art circuit design. One of the architectures is widely recognized to use a single conversion type with a RF front-end, Mixer, IF filter and Image Rejection Filter (IMRF) blocks. This paper focuses the IMRF to be suitable for digital/analog TV signal receptions and multiple IF frequencies. In this circuit topology, a poly-phase filter using on-chip passive components is generally used because of the ease of integration. Due to the limitation of its image rejection ratio (IMRR), especially to a phase/gain mismatch, it has to be adjusted or provided with extra functions to be tuned and/or improved IMRR. To date an improvement of IMRR has mainly been discussed in most papers. In this present work, an issue of distortion, especially for IIP3 performance is resolved as well as tuning method of IMRF.

2. System/Circuit Design
A. Image Rejection Filter Concept
Wideband signal suppression with a certain bandwidth centered at image frequency is required in case of digital TV signal reception. The bandwidth is typically 6MHz in Japan/U.S and 8MHz in Europe/China. This target reflects the filter design concept as shown in Fig.1. It has two stages of poly-phase RC low pass filter with voltage buffers on each signal path. It is divided into three frequency regions for each corner frequency of low pass filter to cover entire bandwidth to be attenuated image signal components. Fig.2 shows an entire block diagram of TV tuner IC including most functions. Note that IF filter is placed before IMRF block on purpose to minimize I/Q phase error with a coarse/fine-tuning of its center frequency to be better IMRR. Maintaining I/Q errors within +/-0.5 degrees at IF filter is expected to achieve at least more than 40dB IMRR. Provided minimum 20dB attenuation of image frequency at RF front-end filters and summing up, overall attenuation is expected to be >60dB, which meets most digital TV tuner system requirement.

B. IIP3 Improvement
Focusing on a signal distortion on TV tuner system, IMRF block is close to the last stage, which can affect the overall IIP3 performance, and it has to be characterized. The IMRF contains 2 sets of buffer stages, which drives next stage of resistor bank and capacitor. The input impedance of 2nd stage depends on the connection of opposite node of each resistor bank, as shown in Fig.1. It should be noted that required drive current of specific frequency at pass band signal varies based on the manner of input impedance. Comparing IM3 performance in Fig.3 between one using buffers with 3mA drive current each and I/Q buffers with different drive current of 1mA and 5mA, 3rd order IM product is improved by more than 20dB. As indicated, total amount of current for both cases are the same, which is 12mA on 2nd stage.

C. Tuning method
Fig.4 shows a block diagram of oscillator block (IMAGE OSC) with a same resistor bank block as used in the IMRF, which is only activated during auto-tuning process [1] to select one set of resistors in the resistor bank by RRR 5bit code. Once the RRR code is determined, the same code is set in the IMRF. This oscillator architecture uses simple positive feedback loop with Auto Level Controlled (ALC) and Limiter (LIM) amplifiers, without any distorted signals into RC filter because of accuracy of oscillation frequency. We designed an oscillator frequency range to be involved a resistor/capacitor tolerance, which covers from ~28% to +32%. Another feature in this resistor bank can set the IF frequencies for multiple countries as such 57MHz in Japan, 44MHz in U.S and 36.125MHz in Europe based on TV standard.

D. Experimental Results
Fig.5 shows a measurement result of IMRR and voltage gain, as related to Japan Digital Channel Frequency. Notice that more than 60dB IMRR is achieved over frequencies in case of maximum gain of 37dB in typical case. Fig.6 shows the oscillation frequency data in the present work. The noticeable difference of tuning range at Japan mode is believed to be due to the parasitic capacitors and resistors on a metal routing of layout, which is 9% narrower than the target. However, image frequency attenuation is widely covered even if the tuning frequency is shifted from the desired RRR code. Resultant data of overall IIP3 at maximum gain, which is around 94dBµV as shown in Fig.5, proves that the IMRF no longer affects any distortion into this system because the output signal level is close to 121dBµV, which is limited by the power supply voltage of 3.3V (=121dBµV).

E. Summary
Table-I has furnished the summary of experimental result
of this work. The system/circuit design has achieved required IMRR on the TV tuner system. See Fig. 7 as for the die photo.

3. Conclusions

In the present work, poly-phase RC filter has been implemented to be suitable for the TV tuner system as a function of image rejection filter. The proposed technique resolves the disadvantage of IMRR limitation to be useful for the mass production. Moreover, a high IIP3 performance at this IMRF is contributed to the overall IIP3 characteristics to be outperformed in a TV tuner IC.

Acknowledgements

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References


Fig. 1 R-C Poly Phase Image Rejection Filter

Fig. 2 Simple Block Diagram of TV Tuner IC

Fig. 3 Simulated IM3 Comparisons

Table-1 IMRF Block Summary

<table>
<thead>
<tr>
<th>Process Technology</th>
<th>0.25μm RF-CMOS</th>
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<tbody>
<tr>
<td>Power Consumption</td>
<td>67 mW @3.3V</td>
</tr>
<tr>
<td>Occupied Die Area</td>
<td>0.48 mm² (w/o PLL)</td>
</tr>
<tr>
<td>Tuning Range</td>
<td>JPN Mode: 41.9 to 71.1 [MHz]</td>
</tr>
<tr>
<td></td>
<td>US Mode: 30.9 to 63.5 [MHz]</td>
</tr>
<tr>
<td></td>
<td>EU Mode: 24.3 to 59.5 [MHz]</td>
</tr>
<tr>
<td>IMRR</td>
<td>Overall: 66.6 to 86.3 [dB]</td>
</tr>
<tr>
<td>@IFOUT=57MHz</td>
<td>(93 to 767 MHz at RFIN)</td>
</tr>
</tbody>
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Fig. 4 Image Oscillator Tuning Block

Fig. 5 Voltage Gain/IMRR/IIP3 Measured Data

Fig. 6 Measured IMAGE OSC Tuning Range

Fig. 7 Die photo