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Characteristics and Modeling of Bulk FinFETs for Circuit Application

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1. Introduction

Recently, bulk FinFETs have been considering very promising candidate for future nano-scale CMOS devices [1]. To design high-speed circuits, characteristics of devices considering drain bias (\(V_{DS}\)) and back bias (\(V_{BS}\)) are very important. So, it is strongly required to model threshold voltage (\(V_{th}\)) behaviors of bulk FinFETs considering \(V_{DS}\) and \(V_{BS}\). We have already proposed \(V_{th}\) model based on charge-sharing at low \(V_{DS}\) [2],[3]. However, the \(V_{th}\) model considering \(V_{DS}\) and \(V_{BS}\) in the bulk FinFETs has not been developed.

In this work, the \(V_{th}\) modeling of the bulk FinFETs considering \(V_{DS}\) and \(V_{BS}\) is performed by changing gate height, gate length (\(L_{g}\)), body doping (\(N_b\)), and fin body width, and verified with device simulation [4]. We compare \(V_{th}\) behavior with \(V_{BS}\) of planar MOSFETs and bulk FinFETs and also check full-down speed of both structures with \(V_{BS}\).

2. Device Structure

Fig. 1(a) shows 3-dimensional (3-D) schematic view of the bulk FinFET. \(H_g\) and \(W_{fin}\) represent the gate height and fin width, respectively. The \(S_{SD}\) stands for junction depth of source/drain extensions (SDE). The LDD concentration is \(7 \times 10^{19} \text{ cm}^{-3}\) and has the profile of about dec/5nm. Gate oxide thickness (\(T_{ox}\)) is fixed at 1.5 nm. Fig. 1(b) shows 2-D cross-sectional view of the fin body cut along A-A’ in Fig. 1(a). \(L_{c}=(L-2x_{ds}=L)\) is the effective channel length based on the box channel doping profile [2].

3. \(V_{th}\) Model and Verification

Side-channel of bulk FinFETs has double-gate (DG) nature as shown in Fig. 1(b). The \(V_{th}\) model of DG MOSFETs considering \(V_{DS}\) can be derived directly with only two parameters \((D_0\) and \(D_2\)) from diffusion current model [5] of fully depleted (FD) DG MOSFETs based on surface potential and is given by

\[
V_{th} = V_{th0} - D_0 V_{DS} - D_2 V_{DS}^2
\]

where \(D_0\) is a physical parameter to determine the exponential increment of diffusion current by \(V_{th0}\) and \(D_2\) is a parameter to consider the drain-induced barrier lowering (DIBL). In (1), \(V_{th0}\) [2],[3] is the \(V_{th}\) model of FD DG MOSFETs with doped channel based on charge-sharing at a low \(V_{DS}\).

Fig. 2(a) shows \(D_0\) versus \(V_{DS}\) as a function of \(L_{c}\) for FD DG MOSFET with a \(W_{fin}\) of 15 nm and an \(N_b\) of \(5 \times 10^{18} \text{ cm}^{-3}\). \(D_0\) decreases as \(L_{c}\) decreases or \(V_{DS}\) increases, which is physical. Fig. 2(b) shows \(D_2\) versus \(L_{c}\) as a function of \(W_{fin}\) for FD DG MOSFET with an \(N_b\) of \(5 \times 10^{18} \text{ cm}^{-3}\). As shown in the insert of Fig. 2(b), the \(L_{c}\)’s for \(W_{fin}\) of 15 and 30 nm at a given \(N_b\) of \(5 \times 10^{18} \text{ cm}^{-3}\) are about 110 and 160 nm, respectively. As \(L_{c}\) decreases and/or \(W_{fin}\) increases, \(D_2\) increases because of DIBL increase.

Fig. 3 shows \(V_{th}\) versus \(V_{DS}\) as a function of \(L_{c}\) for doped DG MOSFET with a \(W_{fin}\) of 15 nm. The \(V_{th}\) is represented by solid circle symbols with \(V_{th0}\) extracted by (1). Solid rectangular symbols stand for the \(V_{DS}\) extracted by conventional constant current (CC) method where drain current is fixed at a value at a low \(V_{DS}\). Open triangle symbols represent the \(V_{th}\) extracted by using \(g_{mn}\) method which is known as accurate method. Our model predicts more accurately the \(V_{th}\) behavior with \(V_{DS}\) than the CC method. The error between our model and the CC method increases as \(V_{DS}\) increases and/or \(L_{c}\) decreases.

Fig. 4 shows \(V_{th}\) versus \(V_{BS}\) for planar MOSFET and bulk FinFET with \(L_g=50 \text{ nm}\) and \(N_b=2 \times 10^{18} \text{ cm}^{-3}\) at a given \(V_{DS}=0.05 \text{ V}\). To compare the back bias effect of two devices, \(V_{th}\) of two devices with the same channel width were made equal to 0.35 \text{ V} at a low \(V_{BS}\) by workfunction engineering. Planar MOSFET has a back bias effect as shown in Fig. 4. But bulk FinFET has not a back bias effect for given \(V_{BS}\) from –0.4 \text{ V} to 0.6 \text{ V}.

Fig. 5 shows cross-sectional view of the fin body near the bottom of the gate. The \(x_{ds}\) and \(x_{df}\) are changed by the back bias and represented by the thin dash-dot line and the dashed lines, respectively. The depletion width \(x_{df}\) reflecting narrow width effect (NWE) is given by similar expression to that of conventional back bias effect as follows

\[
x_{df} = x_{df0} \left[ 1 + \left( \sqrt{2} - 1 \right) \left( V_{BS} - V_{th0} \right) \right]
\]

where \(\zeta\) is a factor to consider 2-D charge change with the \(V_{BS}\) and about 0.8 in this case. The \(x_{df0}\) is a value at \(V_{BS}=0\).

Fig. 6 shows \(x_{ds}\) versus \(V_{BS}\) as a parameter of \(N_b\) and \(W_{fin}\). The \(x_{ds}\) for the high \(N_b\) decreases appreciably with increasing \(V_{BS}\). A new model to obtain accurate \(x_{ds}\) with the \(V_{BS}\) is given by

\[
x_{ds} = \frac{2x_{df0}(2V_{th0} - V_{BS})}{qN_b}
\]

where a fitting parameter \(\beta\) is introduced to consider device geometry and about 1.1.

Fig. 7 shows \(V_{th}\) versus \(V_{BS}\) as a parameter of \(N_b\) and \(W_{fin}\). Here, the bulk FinFET has an \(H_g\) of 150 nm and no top corner region. The proposed model shows a good agreement with the simulation as the \(V_{BS}\) increases. The \(V_{th}\) with the negative \(V_{BS}\) is saturated because the \(x_{ds}\) is saturated at 0.5\% of \(W_{fin}\) and the \(x_{ds}\) contribution is negligible compared to that from the side-channel (high \(H_g\)).

Fig. 8 shows \(V_{th}\) versus \(V_{BS}\) as a parameter of \(L_{c}\). Here, the bulk FinFET has a half-circle corner. The \(V_{th}\) is determined by the \(x_{ds}\) and \(x_{df}\). Our model predicted well the \(V_{th}\) behaviors of bulk FinFETs considering back bias.

Fig. 9 shows change of full-down delay time and \(V_{th}\) versus \(V_{BS}\) as a parameter of device structure. The insert illustrates an inverter circuit. Here, supply voltage (\(V_{CC}\)) is 0.9 \text{ V}. The bulk FinFET shows that the delay time does not change with \(V_{BS}\). But planar MOSFET shows delay time increase with negatively increasing \(V_{BS}\) and the delay time increases by about 23 \% at \(V_{BS}\) of –0.5 \text{ V}. This means that the bulk FinFET is more effective device for the full-down circuits which consist of devices connected in series.

4. Conclusions

We have verified that bulk FinFET has negligible threshold voltage change with back-bias compared to planar MOSFET, and modeled the threshold voltage behavior of the fully depleted bulk FinFET with doped channel by considering \(V_{th}\) and \(V_{DS}\). The models were compared with device simulation and explained well the \(V_{th}\) behavior.

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Fig. 1. (a) 3-D schematic view of bulk FinFET. $H_g$ and $W_{fin}$ represent fin height and width, respectively. (b) 2-D cross-sectional view of the bulk FinFET cut along A-A' in (a). $T_{ox}$ and $x_h$ represent the gate oxide thickness and charge-sharing length, respectively.

Fig. 2. (a) $D_0$ versus $V_{th}$ as a function of $L_g$ for fully-depleted DG MOSFET with a $W_{fin}$ of 15 nm. (b) $D_0$ versus $L_g$ as a function of $W_{fin}$ for fully-depleted DG MOSFET with an $N_b$ of $5 \times 10^{18}$ cm$^{-2}$. The insert in (b) represents $L'$ versus $W_{fin}$, $L'$ is the longest channel length with DIBL.

Fig. 3. $V_g$ versus $V_{th}$ as a parameter of $L_g$. $W_{fin}$, $N_b$, and $T_{ox}$ are 15 nm, $5 \times 10^{18}$ cm$^{-2}$, and 1.5 nm, respectively. Here, the $V_g$ data from CC and $G_{max}$ methods were obtained from extensive device simulation.

Fig. 4. $V_g$ versus $V_{th}$ for planar MOSFET and bulk FinFET with $L_g=50$ nm and $N_b=2 \times 10^{18}$ cm$^{-2}$ at a given $V_{DS}=0.05$ V. $V_{DS}$ of two devices are 0.35 V at a $V_{th}$ of 0.05 V.

Fig. 5. 2-D cross-sectional view of the fin body near the bottom of the gate. The $x_{dep}$ and $x_{ds}$ are changed by the back bias and represented by the thin dash-dot line and the dashed lines, respectively. The $x_{ds}$ is a value at $V_{th}=0$ V.

Fig. 6. $x_{dep}$ versus $V_{th}$ as a parameter of $N_b$ and $W_{fin}$. The $x_{dep}$ for the high $N_b$ decreases appreciably with increasing $V_{th}$.

Fig. 7. $V_g$ versus $V_{th}$ as a parameter of $H_g$ and $W_{fin}$. Here, the bulk FinFET has a $H_g$ of 150 nm and no top corner region. The model shows a good agreement with simulation.

Fig. 8. $V_g$ versus $V_{th}$ as a parameter of $L_g$. Here the bulk FinFET has a half-circle corner, a $H_g$ of 100 nm, and a $W_{fin}$ of 20 nm. The model shows a good agreement with simulation.

Fig. 9. Change of full-down delay time and $V_{th}$ with $V_{DS}$ as a parameter of device structure. Here, $L_g$ and $C$ are fixed at 45 nm and 20 fF, respectively. The insert illustrates an inverter circuit. The $V_{CC}$ is 0.9 V.

References