Temporal Noise Analysis and its Reduction Method in CMOS Imager Readout Circuit

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I Introduction

Although CMOS imager has many advantages, such as low power consumption and capability of integrating sensor/signal processing circuits in a single chip, its performance is highly limited by the noise of the readout circuit. Noise analysis was performed at dark state since the effect of noise is apparent at low illumination level. Moreover, we included the effect of CDS (Correlated Double Sampling) operation on the output noise voltage. Finally, we will present the noise reduction method by varying transistor sizes.

II Readout Circuit and Analytical Noise Equation

The 4-TR Active Pixel Sensor (APS) readout circuit investigated in this work is shown in Fig.1a. In-pixel devices (M1, M2) are buried-channel type. Cgs is the parasitic p-n junction capacitor of the floating diffusion which relates the photon generated charge signal to voltage signal. Column current source consists of M3, M4, and M5. When transmission gate (M6, M7) turns on, voltage across the sampling capacitor (Cs) tracks the pixel output voltage. As a first step to analyze the output noise, the analytical noise Eq. (1) of the readout circuit was derived by using the associated small signal equivalent circuit shown in Fig.1b.

\[
\Delta V_{\text{noise}} = \sum_{i} H_{i}(s) \Delta V_{i}
\]

where

\[
R_{q} = \frac{1}{R_{s} + R_{d}} + \frac{1}{R_{eq} + R_{short}}
\]

\[
I_{q} = \frac{1}{R_{s} + R_{d}} \frac{R_{eq} + R_{short}}{R_{eq} + R_{short}} I_{p}
\]

Fig.2 shows that transfer functions from derived equation agree well with the simulation results and thus validates Eq. (1).

III CDS Operation and its Effect on Output Noise Voltage

Portion of the CDS circuit and its timing diagram is shown in Fig.3. At reset sampling (phase 1) since input and output of the inverter is shorted, node IN sets to the switching threshold voltage. (typically $V_{DD}/2$) Therefore, reset level is sampled on a capacitor with capacitance of C0+C1. After transferring signal charge to the floating diffusion capacitor (phase 2), reduced pixel output voltage is sampled as a signal sampling (phase 3). In this phase, notice that node IN is at floating state, so the reduced pixel output is sampled on a capacitor with capacitance of C1. At the end of phase 3, node IN will deviate from switching threshold by the same amount of reset level subtracted from the signal level. Following circuits, including the inverter, process this deviation value of node IN, and convert it to digital data.

We mentioned that the sampling capacitor (Cs in Eq.1) during reset and signal sampling phase have different capacitance values which affects denominator of the transfer function (Eq.1). Therefore, the deviation voltage of node IN due to transistor noise, which is the output noise voltage with CDS effect considered, can be expressed by Eq.(2). $T_{r}/2 = (1/2f_{c})$ is the interval between two sampling points. Eq.(2.b) is the associated power spectral density expression obtained from Eq.(2.a).

\[
\Delta V_{\text{noise}}(f) = V_{\text{noise}}(f) - V_{\text{noise}}(0) = \sum_{k} (H_{k}(f) + f_{s}/2) - H_{k}(f) f_{s} \Delta f_{k} S_{f \cdot k} (2.a)
\]

\[
S_{\Delta V_{\text{noise}}}(f) = \sum_{k} |H_{k}(f)|^{2} f_{s} \Delta f_{k} S_{f \cdot k} (2.b)
\]

IV Results and Discussion

Previously, we derived channel thermal noise as an integral form [1]. By using short channel current expression, the integral form can be expressed as

\[
S_{\Delta V_{\text{noise}}}(f) = 4kT \cdot f_{s} \int (f_{D} + 1/E_{c}) (3)
\]

Eq.(3) which is valid for both linear and saturation regions was used to obtain the thermal noise component of the CDS affected output noise voltage PSD (Power Spectral Density) by Eq.(2.b). Low frequency noise is composed of flicker noise and RTN (Random Telegraph Signal Noise). Due to its randomness nature, RTN in a specific device can only be quantified from measurement. Consequently, several nominally identical samples were selected from the wafer for each of the transistors in Fig.1 to measure the Lorentzian shaped RTN PSD. Fig.4 illustrates an example of extraction method of RTN and flicker noise PSD out from the measured raw data. By using the fitting parameters obtained from the fitting tool, both for flicker noise and RTN, we can evaluate the low frequency noise component of the CDS affected output noise voltage PSD from Eq.(2.b). Integrating the CDS affected total output noise voltage PSD (S_{\Delta V_{\text{noise}}}) from 0 to infinity, total output noise variance is obtained.

Fig.5 shows the root mean square output noise voltage of each noise components in the readout circuit. We can see that thermal noise of M4 overweights the other noise components. This result is in contrast to the generally known fact that low frequency noise of the source follower dominates other noise sources [3]. The usage of the buried type in-pixel devices [2] and the effect of CDS operation on the RTN (reduces noise power) [4] and thermal noise (doubles noise power) might be the reason for such discrepancy. Actually the average RTN of the source follower before and after CDS operation was calculated to be 78.5 μV, 19.2 μV, respectively. Also the fact that transfer function of M4 is larger than that of M1 can be the reason. Preferably, thermal noise dominant result of this study is thought to represent the majority of the pixels in the imager [5] since the number of the samples used to measure the low frequency noise was not sufficient statistically. By knowing this quantified output noise components, we can select the appropriate transistors to vary the dimensions of its width and length for total noise reduction. Since the thermal noise components of M1 and M4 take up about 85% of the total output noise, a method that reduces the sum of M1 and M4 thermal noise will also reduce the total output noise. We can readily observe from Fig.6 and Fig.7 that each directions for sizing L1, W4, L4 which reduce the output thermal noise voltage of M1, M4, M4 respectively, is same with that to reduce the total output noise voltage. However, sizing W1 shows somewhat complicated behavior of M1 thermal noise voltage. This is because as W1 increases, transfer function of M1 decreases through the increased transconductance parameters in the denominator (Eq.(1)) whereas the thermal noise source tends to increase. Moreover, as W1 increases, output thermal noise voltage of M4 slightly decreases due to its transfer function reduction, and this component can explain the behavior of total output noise voltage.

V Conclusion

Output noise voltage components of the CMOS imager readout circuit has been quantified considering the effect of CDS operation. Thermal noise of M4 is the dominant noise component. Increasing W1, L1, L4 and decreasing W4 reduce the total output noise voltage. However, not much reduction is achieved for W1 larger than 0.25 μm and the optimum L1 was 0.5 μm in terms of input referred noise.

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Fig. 1. Readout circuit and its small signal equivalent circuit investigated in this work. Switches operate in linear region while source follower (M1) and the cascode current source devices (M3, M4) are in saturation region.

Fig. 2. M6 is ignored since it is in cutoff region at dark state.

Fig. 3. CDS circuit and its timing diagram. S1 corresponds to M6 and M7 in Fig. 1.

Fig. 4. Flicker noise and RTN PSDs can be extracted by fitting tool from raw data (a) and two RTN PSDs with different Lorentzian spectrum can be extracted by fitting tool from raw data (b).

Fig. 5. Thermal and low frequency noise components of M3 transistor was negligible due to its extremely low transfer function value at dc. Total output noise voltage is calculated to be 260 μV.

Fig. 6. Thermal noise voltage variation as a function of width and length. Since M1 is inside the pixel, size variation interval is smaller than M4.

Fig. 7. Total output noise voltage variation as a function of width and length. Slopes at the points of the standard (initial) size are shown. According to the slope values, we can say that L1 is the most sensitive geometry to the total output noise voltage at standard size. Input referred noise as a function of W4, L4 are not shown since the size of M4 has negligible effect on the charge to voltage conversion gain. Input referred noise as W4, L4 variation simply follows the total output noise voltage.