A CMOS Image Sensor with CDS and Global Shutter for Three-Dimensional Image Processing System

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1. Introduction

A high performance image processing system with small size image sensor is highly required in various fields such as robot vision systems [1] and automotive applications. These applications require both high speed and high sensitivity in image processing operations. Although the vision chips using the pixel level parallel processing was proposed [2], it is difficult to satisfy both requirements simultaneously because of the large pixel size. The low fill-factor, the area ratio of Photo Diode (PD) in the pixel, causes the low sensitivity.

We have proposed a parallel image processing system LSI with three-dimensional structure to solve these problems [3]. The proposed three-dimensional LSI can satisfy both requirements by adopting the block parallel architecture and Through Si Via (TSV) connecting each stacked layer. Three-dimensional architecture is scalable and can realize the vertical block parallel processing.

Another requirement for high-speed operation is global shutter. Using global shutter, high speed imaging for moving objects is realized without any mechanical shutter. Though CMOS image sensors with global shutter were proposed for the automotive application [4], Correlated Double Sampling (CDS) technique [5] can not be implemented at the same time.

In this paper, a pixel circuit, which realizes the global shutter and the CDS circuit simultaneously, is proposed for the practical design of the CMOS image sensor with three-dimensional structure. Also, design of a prototype chip with the proposed pixel circuit is described.

2. Three-Dimensional Image Processing System

Figure 1 shows a configuration of the proposed parallel image processing LSI with three-dimensional structure. The proposed system consists of an array of CMOS image sensors, A/D converters, frame memories, and processing elements (PE), on each layer. Each layer is vertically stacked and electrically connected using TSVs. The three-dimensional structure can also improve the processing speed by the block parallel processing. Consequently, the three-dimensional structure realizes the scalable parallel architecture for high speed image processing system.

3. Pixel Circuit for Global Shutter and CDS

The cross sectional view of the proposed CMOS image sensor with three-dimensional structure is shown in Figure 2. The image sensor layer and A/D converter layer are connected by TSVs which penetrate the image sensor layer. However, the area of the TSVs cut the side of PD areas, because the TSVs and the PD can not be overlapped. While the pixel size of the contemporary CMOS image sensor for a digital still camera is less than 5×5µm², an assumption of the TSV is currently 3µm of diameter [6]. Therefore, the TSV must be shared by the multiple pixel circuits such as eight pixels to reduce the circuit area.

The configuration of the proposed pixel circuit is shown in Figure 3. The proposed pixel circuit consists of the eight three transistor pixel circuits, pixel select transistors, a coupling capacitor (C_CP), sample hold capacitors (C_HOLD), sample hold select transistors corresponding to each pixels, and an output amplifier. The line between the pixel select transistors and the coupling capacitor C_CP is assumed at the TSV. The signal voltages (V_REF) from the first layer pixel circuits are stored into the sample hold capacitors through the coupling capacitor. Storing the signal voltage into the sample hold capacitors, the global shutter is realized.

In addition, the proposed pixel circuit can correct the fixed pattern noise (FPN) referred to the source follower amplifier and the reset transistor on the pixel circuit using a CDS circuit. The reset voltage (V_REF) is subtracted from the signal voltage on the sample hold capacitor. This pixel level CDS circuit realizes both global shutter and FPN reduction simultaneously. The sampled voltage (V_SP) is obtained as following formula (1), V_REF stands for the reference voltage.

\[ V_{SP} = V_{REF} + \frac{C_{CP}}{C_{SH} + C_{CP}} (V_{RES} - V_{SIG}) \] (1)

From this equation, it is clear that the sampled voltage V_SP stands for the difference of the reset voltage and the signal voltage. Therefore, FPN reduction for each pixel can be successfully carried out. Because of the variation of the output amplifier from the sample hold capacitor to the A/D converter, there is another FPN depending on the pixel block. To overcome this problem, we have implemented a digital domain CDS technique on each A/D converters.

Figure 4 shows an operation timing diagram of the eight pixel circuits. However, the shared TSV is used in turn, therefore the exposure period has a little difference among corresponding pixels. Since the sample hold operation is several clock cycles for each pixel, the differences of the exposure time among eight pixels are relatively smaller than the total exposure time. Consequently, the global shutter and FPN reduction with the CDS circuit can be realized simultaneously.

With the three-dimensional structure, the three-transistor pixel circuit, and the pixel select transistor are placed on the first layer, and lest of the components are placed on the second layer. Though the area of proposed pixel circuit is larger than the area of conventional pixel circuit of the CMOS image sensor, this problem can be relieved by using three-dimensional structure.

4. Performance Evaluation of proposed the pixel circuit

To evaluate the proposed pixel circuit, a prototype of the CMOS image sensor is fabricated with the conventional two-dimensional standard CMOS technology. A die photograph of the designed chip is shown in Figure 5. Specifications of the prototype chip are shown in Table 1. The designed chip consists of a 32×32 pixel array, parallel A/D converters, a control circuit, and TEG circuits. The pixel array consists of 128 blocks of the
eight pixel circuits as shown in Figure 3. To realize the CMOS image sensor with three-dimensional structure, the A/D converters must be placed under the pixel circuit for block parallel structure. However, in this design, the column parallel structure is used because of the conventional two-dimensional technology. Therefore, appropriate architecture of the A/D converter must be considered with the three-dimensional structure.

The performance evaluation of the pixel circuit was carried out using the prototype chip. Figure 6 shows the photovoltaic conversion characteristics on the output conversion voltage for the two integration times. From this result, the photovoltaic conversion is performed correctly. In addition, the output voltage swing is about 600 mV, which is enough to operate the 8 bit A/D conversion. The prototype chip is operated at 3.3 V.

5. Conclusion
In order to realize the small and high-speed image processing system, we proposed the practical design of the CMOS image sensor with three-dimensional structure and evaluated pixel characteristics by photovoltaic conversion experiments.

The proposed pixel circuit realizes the global shutter and the CDS operation simultaneously by using the pixel level CDS. To evaluate the proposed pixel circuit, we designed the prototype of the CMOS image sensor with the conventional two-dimensional standard CMOS. From the evaluation results, we confirmed that the proposed pixel circuits can operate with the pixel level CDS and global shutter.

References

Table 1. Specifications of designed CMOS image sensor

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<thead>
<tr>
<th>Process Technology</th>
<th>0.13 μm CMOS, Double Poly-Si-L</th>
<th>4-Metal</th>
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<td>Chip Size (mm x mm)</td>
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<td>Supply Voltage (V)</td>
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<td>Operating Frequency (kHz)</td>
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<td>20</td>
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<td>Number of Pixels</td>
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<td>20 x 12</td>
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<tr>
<td>Fill Factor (%)</td>
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<td>50</td>
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</table>

Fig. 1. Proposed high speed image processing system with three-dimensional structure.

Fig. 2. Cross sectional view of image sensor with three-dimensional structure which has shared TSV.

Fig. 3. Configuration of proposed pixel circuit.

Fig. 4. Operation timing of proposed pixel circuit.

Fig. 5. Photograph of prototype chip.

Fig. 6. Photovoltaic conversion characteristics.