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Self-Assembly for Heterogeneous Integration with Lateral Interconnections Extending over MEMS and LSI Chips

Takayuki Konno[1], Takafumi Fukushima[1], Risato Kobayashi[1], Tetsu Tanaka[1, 2], and Mitsumasa Koyanagi[1]

[1] Department of Bioengineering and Robotics, Graduate School of Engineering, Tohoku University
6-6-01 Aza-Aoba, Aramaki, Aoba-ku, Sendai, Miyagi, 980-8579, Japan.
Phone: +81-22-795-6906; Fax: +81-22-795-6907; E-mail: sdlab@sd.mech.tohoku.ac.jp
[2] Department of Biomedical Engineering, Graduate School of Biomedical Engineering, Tohoku University

1. Introduction

Heterogeneous integration combining MEMS with LSI has recently been of great interest due to its high functionality and potential application. In order to realize highly integrated Si interposers, printed wiring boards (PWB), and flexible printed circuits (FPC), we have developed new technologies such as high-throughput multi-chip assembly, lateral interconnection formation extending over chips, high density microbump formation, and passive device fabrication. Figure 1 shows a conceptual viewgraph of a highly integrated heterogeneous system we proposed. Conventional multi-chip modules (MCM) are produced by robotic pick-and-place techniques that enable to sequentially assemble known good dies (KGDs) onto a substrate one by one. On the other hand, fluidic self-assembly techniques using surface tension of liquid can provide batch assembly of a large number of small devices. [1] In addition, both high-precision chip alignment and room-temperature direct bonding can be simultaneously accomplished in our self-assembly technique. We have previously reported the self-assembly for 3D integration with through-Si vias (TSVs). [2], [3] This paper demonstrates the self-assembly of anisotropically etched Si chips targeting for MEMS such as acceleration sensors and passive devices such as coils, and also discusses several parameters related to alignment accuracy and bonding strength of the self-assembled chips.

2. Experimental

Process sequences for test chip/substrate fabrication and our self-assembly process are schematically shown in Fig. 2. 140-μm-thick test chips with a cavity (1-mm- or 2-mm-square in a side) were resulted from thermally oxidized Si wafers by standard photolithography techniques and the subsequent anisotropic etching with 25 % tetramethylammonium hydroxide (TMAH) at 70 ºC, followed by deep reactive ion etching (RIE) to create precisely defined 2-mm- or 3-mm-square chip sizes. These chips have hydrophilic bonding areas at the backside. The substrates for chip assembly were also formed with thermally oxidized Si wafers. A number of plateaus with channels were formed on the substrates by RIE. The plateau surface is rendered hydrophilic to facilitate direct bonding in the following self-assembly using aqueous liquid. The bonding areas of the chips have the same size to the plateau surface area except for the area of the channels through which water in the aqueous liquid can evaporate. In the self-assembly operation, first, the aqueous liquid ranging from 0.2 to 0.4 μL was dropped onto the hydrophilic plateau surface. Then, the test chips having the hydrophilic backside were roughly aligned and placed onto the hydrophilic plateaus with channels. After liquid evaporation, the chips were bonded on the plateaus formed on the substrates at room temperature without applying load to the chips.

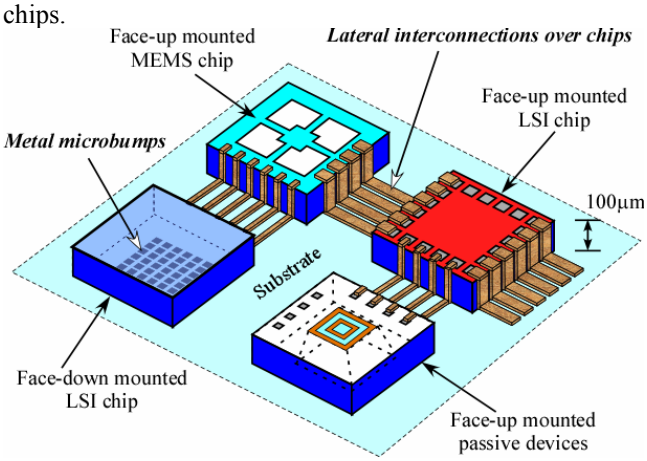

Fig. 1 Conceptual viewgraph of a highly integrated heterogeneous system with lateral interconnections extending over MEMS and LSI chips.

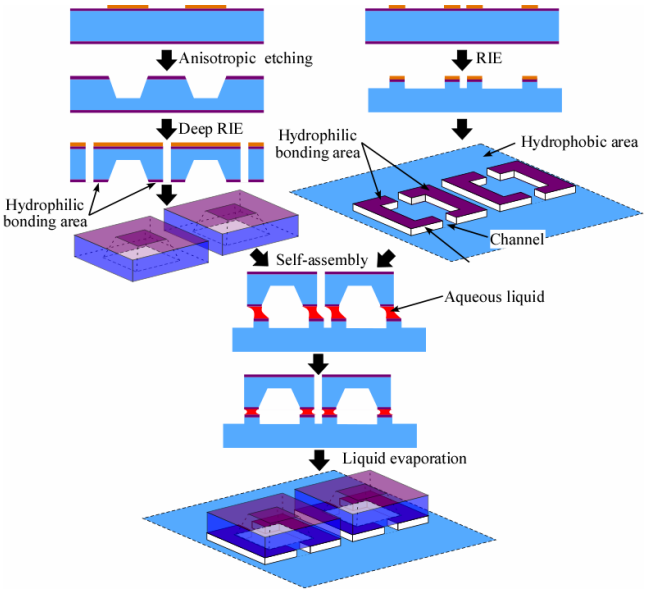

Fig. 2 Process flows for fluidic self-assembly of test chips with a cavity onto plateaus with channels formed on a Si substrate using aqueous liquid.

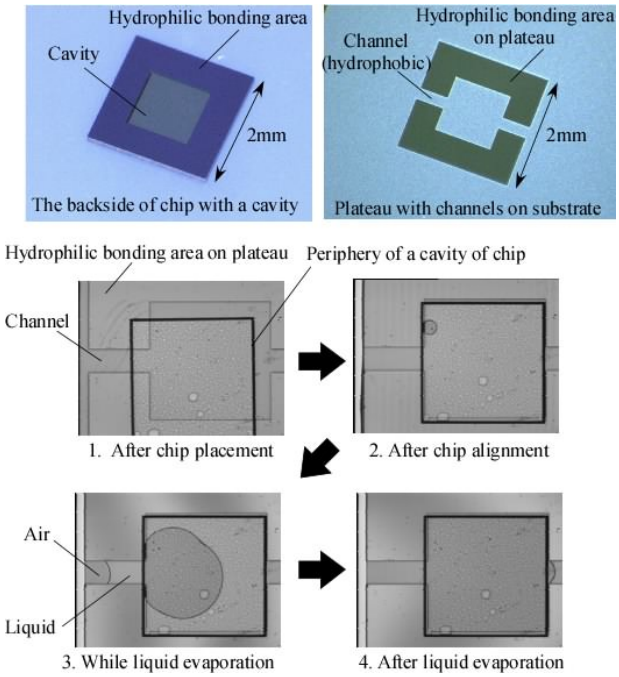

Fig.3 Photomicrographs of the backside of a test chip with a cavity and the surface of a plateau with channels, and frames from video of a self-assembly event (including liquid evaporation through the channel) taken with IR microscope.

3. Results and discussion

The photomicrographs of the resulting anisotropically etched chip with a 1-mm-square cavity and a plateau formed on a substrate are shown in Fig. 3, where self-assembly using the chip and substrate is monitored with IR microscope. As seen from the figure, immediately after chip placement, the chip is driven by surface tension of a small droplet of aqueous liquid, and in addition, the liquid trapped inside of the cavity can be readily removed through a channel: alternatively, air can enter the space between the chip and substrate. This observation indicates that the channels are effective tools to remove liquid from the cavity. Consequently, as shown in Fig.4, many chips with cavities were precisely aligned and tightly bonded onto the bonding areas on the surface of the plateaus with the cavities formed on the substrate.

In general, alignment accuracy on self-assembling depends on wettability contrast between bonding areas and the surrounding background. In our case, the contact angle of the former hydrophilic bonding areas on plateaus is below 10 degree, whereas the latter contact angle is about 70 degree. However, in this study using the plateau structure, the contact angle on the plateau surface strongly depends on liquid volume because the liquid will be confined to the central area. The contact angle is found to be more than 120 degree when 18-μL water is attached to a 3-mm-square plateau. The alignment accuracy is turn out to be approximately 450 nm, as shown in Fig. 5. Higher alignment accuracy can be obtained by the optimization of assembly conditions such as stage inclination and initial positioning error of *X, Y, Z, θ* directions before chip release. Chip and cavity sizes hardly affect the alignment accuracy.

On the other hand, bonding strength is influenced by the surface roughness on the bonding areas. The R_a roughness of the plateau surface was around 1.8 Å from the AFM observation. The high shared bonding strengths of more than 5 MPa, that is enough to allow bulk deformation or edge chipping of thin chips, are obtained under this assembly conditions.

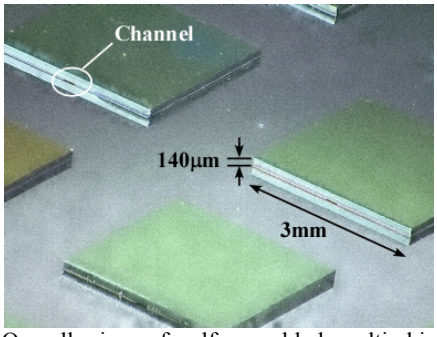

Fig. 4 Overall view of self-assembled multi-chips with a cavity onto plateau with channels on a Si substrate.

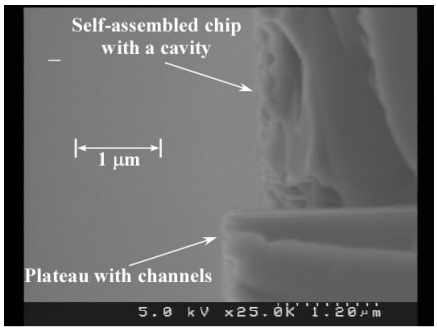

Fig.5 SEM cross-sectional view of a self-assembled chip bonded onto hydrophilic bonding area on plateau surface.

4. Conclusions

Fluidic self-assembly of Si chips with a cavity using surface tension of aqueous liquid is demonstrated to achieve heterogeneous integration with lateral interconnections over MEMS and LSI chips. The aqueous liquid can give the self-assembled chips high alignment accuracy within 500 nm and high bonding shared strength more than 5 MPa. The formation of lateral interconnections extending over large thickness chips will be described in another presentation.

Acknowledgments

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References

[1] H. J. Yeh and J. S. Smith, *IEEE Photonics Technol. Lett.*, **6**, 706 (1994).

[2] T. Fukushima and M. Koyanagi et al., *IEDM Tech. Dig.*, pp. 359-362 (2005).

[3] T. Fukushima and M. Koyanagi et al., *IEDM Tech. Dig.*, pp. 985-988 (2007).