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Modeling of High-Voltage MOSFETs for Device/Circuit Optimization

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Abstract

Specific features of high-voltage MOSFETs and their modeling are summarized based on HiSIM-HV, which has been developed on the basis of HiSIM (Hiroshima-university STARC IGFET Model) for bulk MOSFETs. A consistent potential description across MOSFET channel and high resistive drift region is the characteristic feature of the HiSIM models. The HiSIM-HV model covers symmetric and asymmetric device types up to several 100V switching capability with reproduction of accurate scaling properties of the devices.

1. Introduction

High-voltage MOSFETs are used in many automotive and mobile applications for high voltage switching. The wide range of the operation conditions from a few volts to several hundred volts is realized with a low impurity concentration region, called the drift region. Two major high-voltage (HV) MOSFET types can be distinguished as shown in Fig. 1. The first type is a laterally-diffused asymmetric structure called LDMOS, and the second type is a symmetric structure with drift regions for high-voltage capability at both source and drain [1].

It has been observed that the capacitance of any LDMOS devices shows anomalous characteristics as a function of applied voltages, which has to be modeled accurately for correct prediction of switching performances. Requirements for the drift-region optimization are very high due to its strong influence on LDMOS characteristics. In this paper the compact HV-MOSFET model HiSIM-HV is reported, which was recently selected by the Compact Model Council (CMC) as the industry-standard high-voltage MOSFET model [2]. With HiSIM-HV it is verified, how the anomalous behavior of the LDMOS capacitacnes are related to device structures and other device performances such as transconductance g_m characteristics.

2. Modeling of HV-MOFETs

An important feature of the core model HiSIM2 is shown schmatically in Fig. 2 [3,4]. The Poisson equation is solved at souce side and drain side separately with the quasi-Fermi potential, thus providing the complete potential distribution along the channel down to drain. This is extended to the case with high resistive drain region (see Fig. 3). The potential drop ΔV is calculated as the IR drop with drain current I_{ds} and the resistance in the drift region R_{drift} as

$$\Delta V = I_{ds} * R_{drift} \qquad (1)$$

where R_{drift} is a function of device parameters in the drift region as well as of applied voltages. Circuit simulators recognize the external node potentials, and the device characteristics are described as a function of internal node potentials. However, some device features are determined by both node potentials. This makes modeling relatively complicated. In addition to the above described HV-MSOFET features, the self-heating effect cannot be ignored in HV-MOSFETs. This can be modeled with a thermal RC network consisting of thermal resistacnes and capacitances.

3. Simulation Results

The calculated potential values at the junction, $\phi_s(\Delta L)$ are compared in Fig. 3 with 2D-device simulation results. The anomalous potential characteristics are the origin of all observed LDMOS-MOSFET features. However, as ΔV in the source dominates, these amonalies disappear in the symmetrical HV-MOSFET. If we once have the potential distribution from the source to the drain, we can calculate all device characteristics. Fig. 4 compares the *I-V* characteristics with two different impurity concentrations N_{drift} in the drift region [5]. Fig. 5 shows the gate capacitance C_{gg} comparison for these two cases. The abrupt reduction of g_m and the anomalous spike observed in C_{gg} are both caused by the resistance effect in the drift region.

Fig. 6 compares capacitance values between LDMOS structure and symmetrycal HV-MOSFET [6]. For both cases, C_{gg} shows humps between V_{gs} of 0 and 1V. This is the overlap capacitance contribtuion, which prevents circuits from achieveing high switching performaince. To ensure high voltage blocking capability of a HV-MOSFET, a highly resistive drift region is required. However, the high resistivity causes degradation of the device performances. This is the reason for the requirement of total optimization of HV-MISFETs. Fig. 7 verifies predictability of HiSIM-HV for device optimization of the drift region.

Acknowledgements

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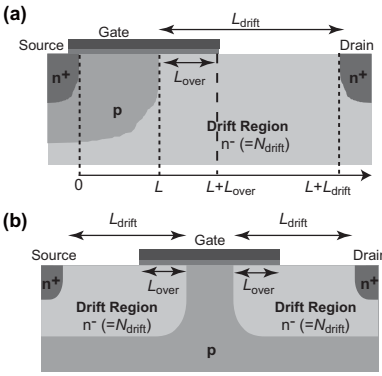

Fig. 1. Cross-sections of the LDMOS (a) and HVMOS (b) high-voltage MOSFET devices.

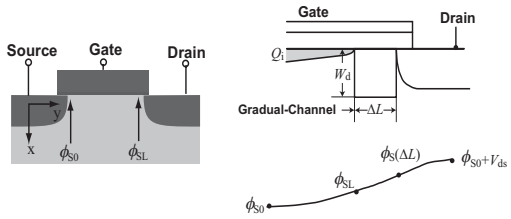

Fig.2. Important surface potentials calculated in HiSIM2 for the bulk MOSFET.

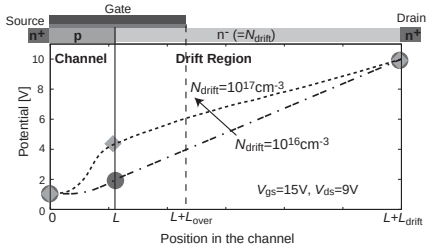

Fig. 3. Calculated potential distribution along the channel with HiSIM-HV (shown with symbols) for two N_{drift} concentrations.

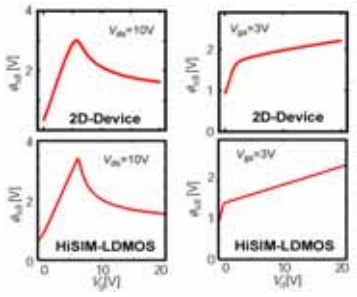

Fig. 4. Potential values at the channel/drift junction ϕ_{sdl} as a function of gate voltage V_g and drain voltage V_d in comparison to 2D-device simulation results.

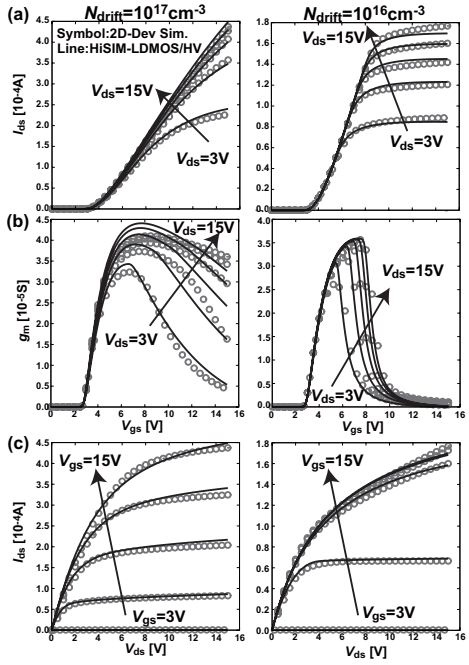

Fig. 5. *I-V* and g_m comparison between 2D-device simulator (symbols) and HiSIM-HV (lines) for the LDMOS structure with different drift-region doping of 10^{17}cm^{-3} (left) and 10^{16}cm^{-3} (right).

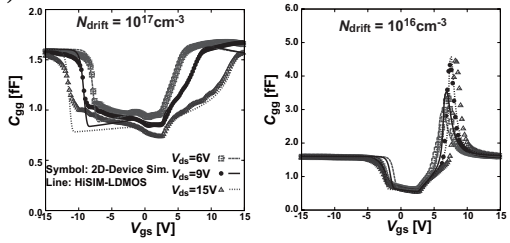

Fig. 6. C_{gg}-capacitance comparison between 2D-device simulation (symbols) and HiSIM-HV (lines) for the LDMOS structure with different drift-region dopings.

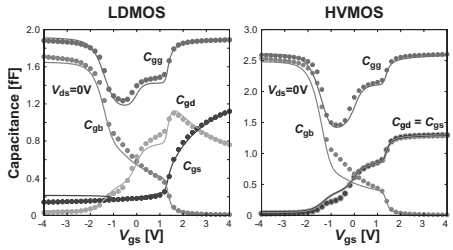

Fig. 7. Capacitances calculated for the LDMOS and symmetric HV-MOS structures with HiSIM-HV (lines) and 2D-device simulation (symbols).

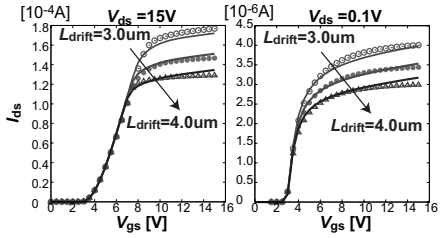

Fig. 8. Scalability of HiSIM-HV with drift-region length L_{drift}. The plots show the I_{ds}-V_{gs} characteristics at high and low drain bias in a comparison of 2D-device simulation and HiSIM-HV results.