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Optical configuration using a silver-halide holographic memory including four configuration contexts

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I. Introduction

Optically reconfigurable gate arrays (ORGAs) have been developed that combine a holographic memory and an optically programmable gate array VLSI [1], [2]. Contexts of the gate array are stored in a holographic memory; they are optically read out and optically programmed onto the gate array VLSI through photodiodes. Such ORGA architectures present the possibility of providing a virtual gate count that is much larger than those of currently available VLSIs.

Nevertheless, although a large virtual gate count can be realized using the large storage capacity of a holographic memory, the actual gate count, which is the gate count of a programmable gate array VLSI, is important to increase the instantaneous performance of ORGAs. The real gate counts of conventional ORGA-VLSIs are too few because its static configuration memory to store a single configuration context consumes a large implementation area of the ORGA-VLSIs [3].

Therefore, to realize a high-gate-count ORGA-VLSI, Dynamic Optically Reconfigurable Gate Arrays (DORGAs) were proposed: they use the junction capacitance of photodiodes as dynamic memory, thereby obviating the static configuration memory [4]. A 51,272 gate count DORGA-VLSI [5] has been reported.

So, this paper presents a practical demonstration of the DORGA architecture using a silver-halide holographic memory including four configuration contexts. The performances of the DORGA architecture, in particular the reconfiguration context retention time, were analyzed experimentally.

II. Holographic memory recording system

Figure 1 shows a multi-context holographic memory recording system. A He-Ne laser was used as a light source; its respective power and wavelength were about 20 mW and 632.8 nm. The laser light was collimated and the parallel light beam was divided into two parallel beams: a reference beam and an object beam. The object beam is incident to a liquid crystal television panel that displays a configuration context. The intensity distribution of the configuration context is made for the outgoing beam through the liquid crystal television panel and the first polarizers. The outgoing beam's light intensity is adjusted appropriately using the second polarizer. On the other hand, the reference beam is incident to a holographic memory after adjustment of the intensity through two polarizers. Here, the distance between an ORGA-VLSI and a holographic memory was designed as 100 mm. In turn, different contexts are displayed on the liquid crystal television panel and can be programmed respectively onto the upper-left shift area, the upper-right shift area, the lower-left shift area, and the lower-right shift area of a holographic memory. However, in this experiment, an AND circuit was programmed onto four areas. The photograph of a recorded holographic memory is shown in Fig. 2. Here, the silver-halide holographic memory is PFG-01

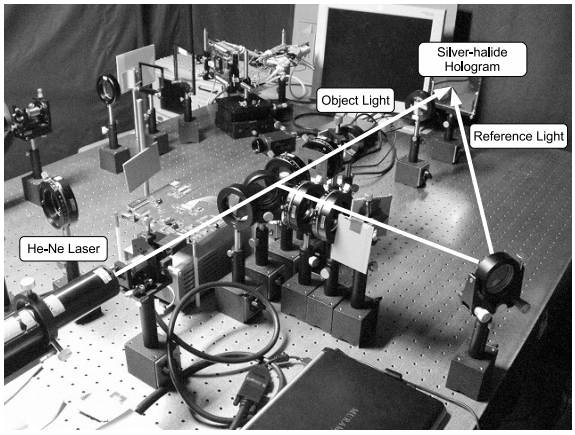


Fig. 1. Recording system for a silver-halide holographic memory.

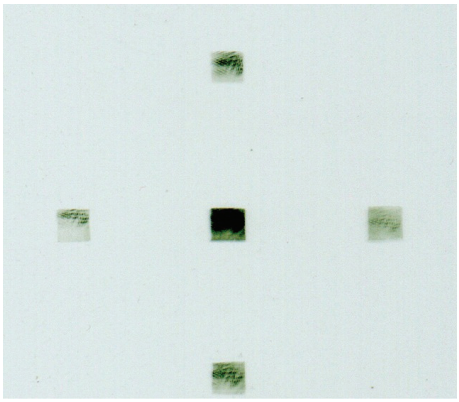


Fig. 2. Recorded holographic memory.

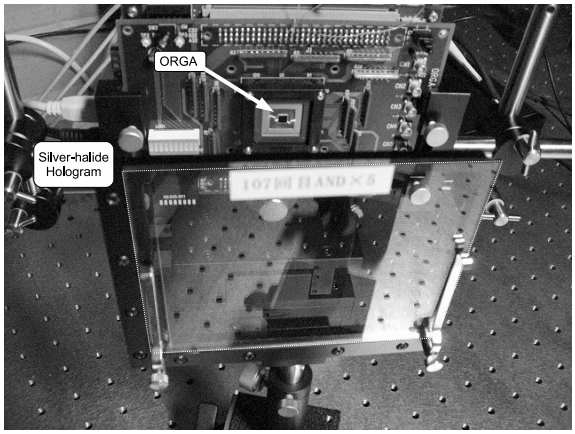
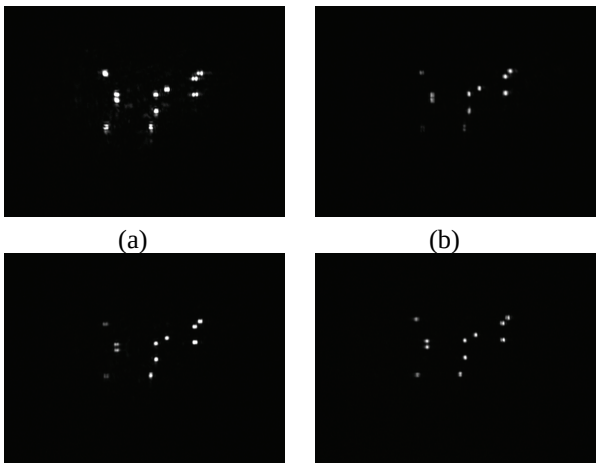


Fig. 3. Reconfiguration experiment.



(a) (b)

(c) (d)

Fig. 4. CCD captured image of an AND circuit context. (a) A context of top hologram. (b) A context of left hologram. (c) A context of ander hologram. (d) A context of right hologram.

silver film (Chuo Precision Industrial Co., Ltd.). The hologram material is 12.7 cm $\times$ 10 cm. The coating thickness of the hologram material is 6–7 μm. The recording particle size is less than 40 nm.

III. Reconfiguration System

A perfect DORGA holographic memory system was constructed using a silver-halide holographic memory and a He-Ne laser as a light source. The respective power and wavelength of the He-Ne laser are about 20 mW and 632.8 nm. The laser light was collimated and the beam is incident to the silver-halide holographic memory including four areas corresponding to four configuration contexts, the size of which is 2 mm $\times$ 2 mm. An ORGA-VLSI chip using the 0.35 μm triple-metal CMOS process was used. The ORGA-VLSI chip includes four logic blocks, five switching matrices, and 12 I/O bits. In all, 340 photodiodes were used to program the gate array. The photodiode size and distance between photodiodes was designed to be 25.5 $\times$ 25.5 μm^2 and as 90 μm to facilitate the optical alignment.

IV. Experimental results

Using that previously described experimental system setup, reconfiguration procedures were executed. Figure 4 shows the diffraction pattern from each area of a recorded holographic memory full adder circuit from the holographic memory, which was recorded at the ORGA-VLSI position using a CCD camera. Under such a condition, a reconfiguration procedure of the full adder circuit was executed. The implementation was successful. The reconfiguration period and retention time were measured respectively as 16 - 58 ms and 15 - 100 ms. The results clarified that the photodiode memory function can retain its state for a long time, as though it were an DRAM, in the case of using a silver-halide holographic memory.

V. Conclusion

This paper has presented a practical demonstration of the DORGA architecture using a high-resolution holographic memory including four configuration contexts. Each recording area of a silver-halide holographic memory is limited to 2 mm $\times$ 2 mm area. The reconfiguration period and retention time were measured respectively as 16 - 58 ms and 15 - 100 ms. The retention time is a longer period than that provided by current available DRAMs. This experimental result shows that the architecture is very useful, even in cases using such high-resolution silver-halide holographic memory. This experimental result presents the attractive possibility of future ORGA with a huge number of contexts.

VI. Acknowledgments

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