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Tapered Through-Si Via Formation for Optical Interposer with 3D ICs and Buried Vertical-Cavity Surface-Emitting Laser / Photo Diode Chips

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1. Introduction

Optical interconnections have been applied to long-distance telecommunication industries for many years. However, there are recently growing requirements to increase bandwidth and density for chip-to-chip or module-to-module interconnects in high-performance computing systems. As the increase in the data transmitting speed, the problems such as cross-talk noise, jitter, and electromagnetic interference (EMI) become more serious for electrical circuits. To overcome these problems, optical interconnections instead of the electrical ones have been studied by lots of companies, organizations, and academies [1]-[3]. Although a large number of optical architectures were proposed, most of them have not yet solved two big problems. One is precise passive alignment between optical waveguides and vertical-cavity surface-emitting laser diodes (VCSELs) / photo diodes (PDs). The other problem is the difficulty in integrating VCSEL chips on LSI chips due to its low compatibility with such GaAs compound devices and complementary metal oxide semiconductor (CMOS). We have addressed the problems to employ "optical interposer" that is a new Si interposer with buried VCSEL / PD chips using polynorbornene (PNB) optical waveguide [4]. In this paper, we mainly describe the formation of tapered through Si-vias (TSVs) and implementation of the optical interposer with the TSVs connected to VCSELs buried in a Si substrate.

2. Concept of Optical Interposer

Figure 1 shows the configuration of parallel processor system with 3D LSI chips and cross-sectional structure of our optical interposer. PNB waveguides optically connect between the 3D LSI chips. In this system, high-accurate alignment of VCSELs to the waveguides can be achieved by cavities formed in a Si substrate and solder bumps. The cavities assist to mount VCSEL / PD chips onto correct positions because the cavity sizes slightly larger than the VCSEL / PD chips are defined by photolithography processes and the chips are readily installed in the cavities. In addition, VCSEL / PD chips can be self-assembled with solder by surface tension of a molten solder. Therefore, the laser emitting apertures and the optical windows of PD are precisely aligned at the designed points. Moreover an insertion loss of the optical interposer can be minimized because of very short distance between PNB optical waveguide and VCSEL / PD chips, and extremely low optical loss of PNB optical waveguide with 0.03 dB/cm at a wavelength of 850 nm.

3. Formation of Tapered TSV

Tapered via formation is necessary for the subsequent conformal deposition of barrier and metal seed layers. The vias with a straight sidewall fabricated by deep reactive ion

etching (DRIE) make it difficult to uniformly deposit the layers on the bottom and sidewall of the resulting vias by sputtering. In addition, the following copper electroplating process results in trapped voids inside the vias with the straight sidewall. In this work, our tapered vias are fabricated by a novel two-step etching process consisting of the Bosch process and isotropic etching, as shown in Fig.2. First, silicon dioxide (SiO₂) of 600-nm thickness was formed on a Si substrate by thermal oxidation. Then, the SiO₂ was excessively etched by buffered HF after photolithographically patterning of TSVs. After that, the Si was etched to form deep holes by the Bosch process, and then, the Si was isotropically etched with SF₆, O₂, and CF₄ gases. The subsequent thermal oxidation provides conformal deposition of a 600-nm-thick SiO₂ layer on the resulting Si vias. Ta as a barrier layer and Cu as a seed layer were sequentially deposited by sputtering on the SiO₂ layer, followed by Cu electroplating for via filling. After the electroplating, Excess Ta and Cu layers on the surface of the Si substrate were removed by a chemical mechanical polishing (CMP) process. After that, electrical circuits were patterned on the surface of the substrate. The backside of the Si substrate was grinded until the thickness of the substrate decreases to 150 μm. Finally, electrical circuits were patterned again on the backside of the thinned substrate.

4. Results and Discussion

Figure 3(a) and 3(b) show the cross-sectional SEM view of the resulting via after the first and the second etching steps, respectively. The former via has 163 μm in depth and 32 μm in top size and bottom sizes, whereas the latter via has 168 μm in depth, 64 μm in top size, and 34 μm in bottom size. The taper angle of 82 degree was obtained by the second isotropic etching step. By changing the etching time on the first Bosch process and the second isotropic etching, the depth of TSVs and the degree of taper can be almost controlled. As seen from this figure, there is no overhang structure on the top of the via underneath a resist mask. Although unique scallops on the via sidewall were resulted from the Bosch process, the profile of the via sidewall became smooth after the second etching. Therefore, the electrical leakage current can decrease and the dielectric breakdown can be improved. From an SEM observation, Ta and Cu layers were turn out to be conformally formed on the tapered via surface by sputtering. Figure 4 shows a cross-sectional view of two kinds of vias filled with Cu by electroplating. The left via is produced by the Bosch process alone without isotropic Si etching, and thus, a large void inside the resulting straight via can be seen from Fig.4 (a). On the other hand, the right

via is obtained by the use of isotropic Si etching in addition to the Bosch process. As seen from the Fig.4 (b), the resulting void-free tapered via is completely filled with Cu. Figure 5 shows the microphotograph of buried VCSEL / PD chips. A buried VCSEL chip can be operated by tapered TSVs through beam-lead pads with solder. A light signal emitted from the VCSEL chip buried in the chip-size cavity was clearly observed. The I-V curve of the VCSEL through tapered TSVs was shown in Fig.6. The characteristic of the VCSEL electrically connected through the TSVs was almost same as that of a primary VCSEL chip. This result indicates that the optical interposer can perform as a high quality optical interface of 3D LSI.

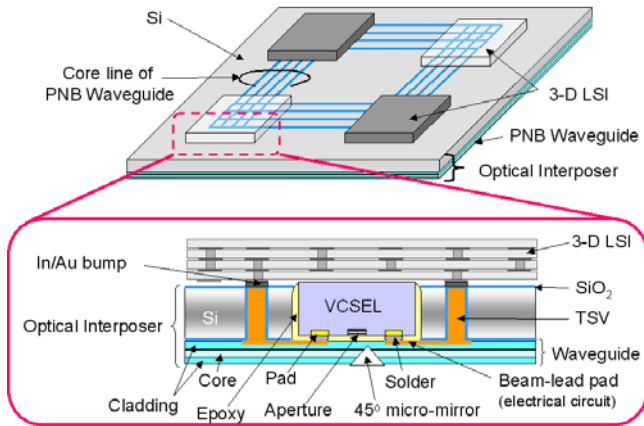


Fig. 1. Parallel processor system with high-performance 3-D LSI chips and cross-sectional structure of optical interposer.

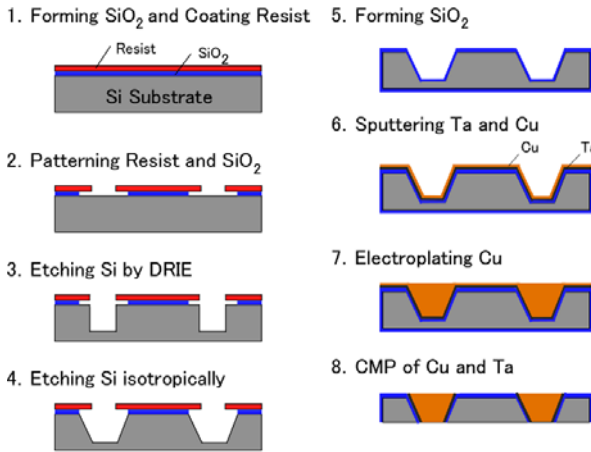


Fig. 2. A novel two step etching process technology for fabrication of tapered TSV.

5. Conclusions

We proposed a novel optical interposer with optical interconnections for a high-performance 3D LSI. A VCSEL chip buried into the optical interposer can be electrically worked through tapered TSVs. In addition, we demonstrated a novel two-step etching for forming the tapered TSVs. The depth and the taper degree of the TSVs can be well controlled by etching conditions. Moreover, the tapered vias were successfully filled with Cu without voids by a DC electroplating.

References

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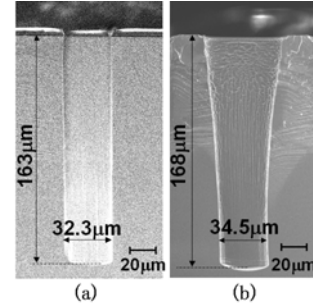


Fig. 3. Cross-sectional SEM view of a via after first etching step (a) and the resulting tapered TSV after second etching process (b).

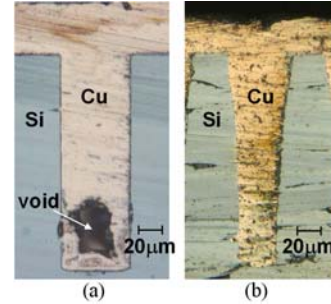


Fig. 4. Cross-sectional view of the via formed by Bosch process (a) and the novel two step etching process (b) after filled by copper electroplating.

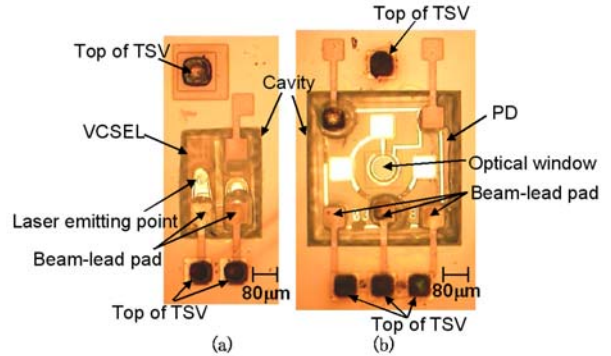


Fig. 5. Microphotograph of a buried VCSEL (a) / PD (b) chip.

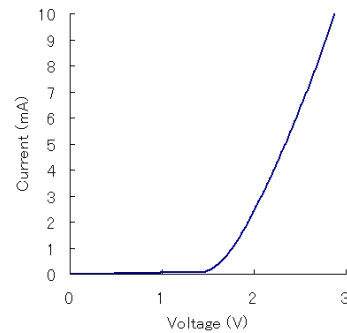


Fig. 6. I-V characteristics of the buried VCSEL.