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Cross-Current SOI MOSFET and Application to Multiple Voltage Reference Circuits

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1. Introduction

One of the authors (Omura) proposed the cross-current tetrode SOI MOSFET (XCT-SOI MOSFET) and examined analog applications [1]. Though the scaling feasibility of XCT-like devices has been studied recently [2], we think XCT devices will yield new applications such as high-voltage devices and SRAM memory cells with high noise margin. In order to assess those applications in sufficient detail, device models are needed to perform circuit simulations. Since Y. Azuma et al. has recently proposed an advanced device model for the XCT MOSFET [3, 4], we are now able to study device applications.

This paper proposes switched multiple-reference-voltage supplier circuits for low-power SOI LSIs. We examine their functions by circuit simulations (*SPICE*) on the basis of measured XCT MOSFET parameters. The usefulness of the XCT SOI MOSFET is demonstrated.

2. Device Structure and Assumptions for Simulations

Schematic device structure is already shown in [1]. In an XCT device, the n-channel MOSFET and p-channel JFET are self-merged and the electron current of the nMOSFET is relayed to the hole current of pJFET in series. The XCT device offers negative differential conductance in the saturation region of drain current [1, 3]; device parameters of fabricated devices are summarized in Table 1. Since the XCT device has active body contact, from pJFET, the body-floating effect is eliminated automatically.

Table. 1. Physical parameters of fabricated devices.

Device parameters	Values	[units]
Nominal body doping, N_A	$1x10^{16}$	[cm^{-3}]
Gate width, *Wn/Wp*	10/20	[μm]
Gate length, *L*	2	[μm]
Gate oxide thickness, t_{ox}	30	[nm]
SOI layer thickness, t_{SOI}	350	[nm]

In circuit simulations, we assume the equivalent circuit for nXCT device as shown in Fig. 1(a). We examined that the equivalent circuit reproduced the I-V characteristics of XCT device. We determined the SPICE simulation parameters using the device parameters shown in Table 1.

3. Proposal of Voltage Reference Circuits and simulation Results

We first propose a two reference voltage circuits, each with one XCT CMOS device, in Fig. 1(b) the XCT devices are shown as equivalent circuits. This is a simple CMOS configuration except for the independent gate terminals of nXCT device and pXCT device. It is assumed V_{DD}=5V and the gate voltage of pXCT device (V_{GP}) basically holds a constant value; threshold voltages are +0.6V for nXCT and -0.6V for pXCT.

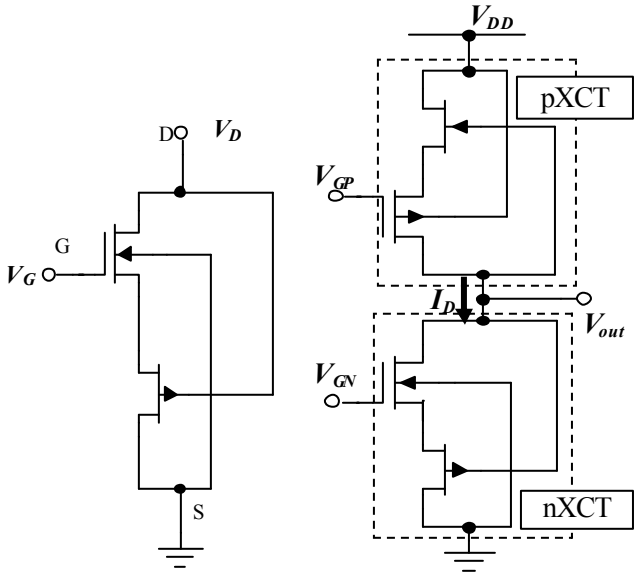

Fig. 1. Equivalent circuit model for nXCT device and XCT CMOS device.

Concept of switching the reference voltage is shown in Fig. 2, where simulated time sequences of the gate voltage of nXCT device (V_{GN}), that of pXCT device (V_{GP}), and output voltage (V_{out}; $V_L \leftrightarrow V_H$). Switching mechanisms are schematically shown in Fig. 3, where the four figures

correspond to notations '(a)' to '(d)' in the time evolution shown in Fig. 2.

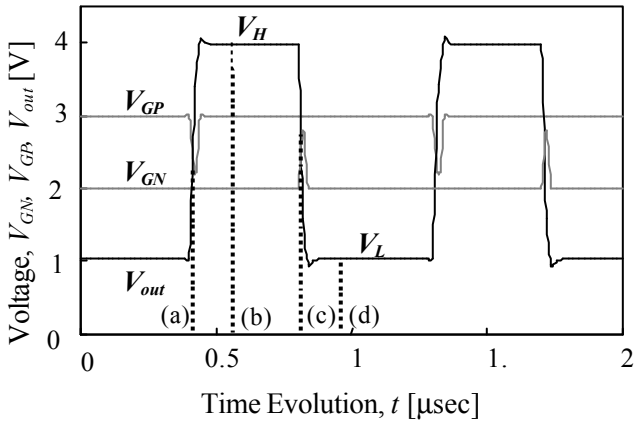

Fig. 2. Time evolution of V_{GN}, V_{GP} and V_{out}.

In the operation shown in Fig. 2, a falling trigger is applied to V_{GP} and a rising trigger is applied to V_{GN}. At the initial stage, V_{DD} of 5V is supplied to the circuit at first, whereupon V_{GN} rises to 2V, and finally V_{GP} rises to 3V; so, V_{out} holds V_L level at the initial stage. In Fig. 2, at t= 0.4 μsec, V_{GP} steps down by 0.8V for a short time and then rebounds, followed by a high V_{out} level (V_H); this process is illustrated in Figs. 3(a) and 3(b). The locus of the cross point of current curves of nXCT and pXCT devices moves from V_L to a certain high level following the sequence shown in 3(a), and it finally t returns to V_H when V_{GP} returns to 3V as shown in Fig. 3(b). At the next stage, V_{GN} rises by 0.8 V at t=0.8 μsec and returns to 2 V; this trigger forces V_{out} to step down to V_L. This sequence is illustrated in Figs. 3(c) and 3(d).

We also propose a three-reference-voltage circuit for practical convenience (not shown here). Basics of the operation mechanism are the same as those illustrated in Fig. 3.

Acknowledgment

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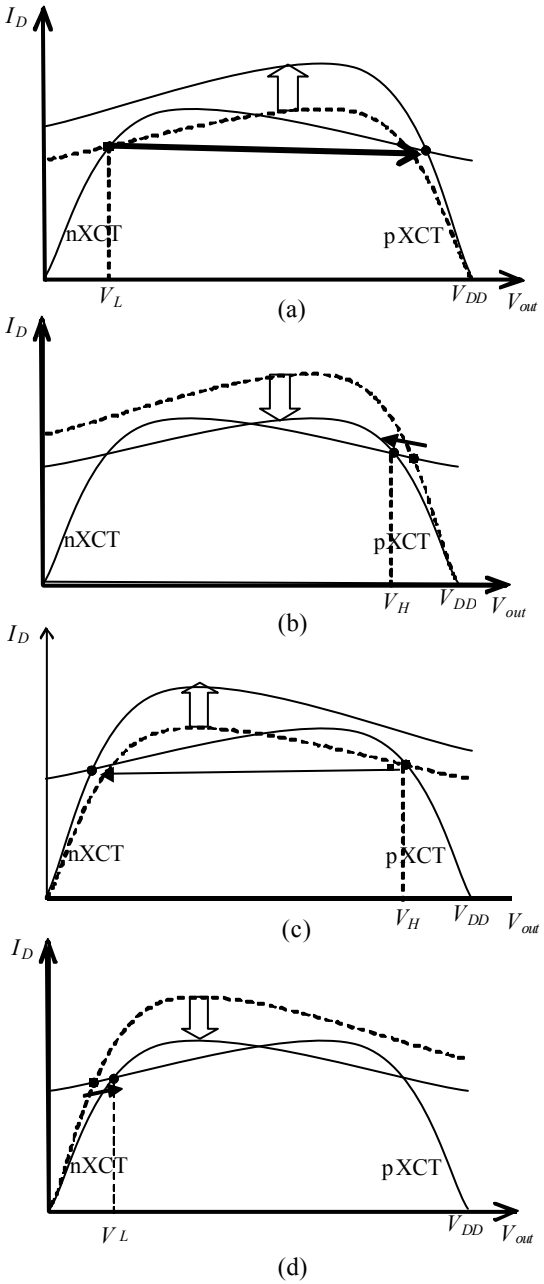

Fig. 3. Switching mechanism of reference voltages.