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Room Temperature Operation of Carbon Nanotube Single-Hole Transistors Fabricated by Shadow Evaporation Methods

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1. Introduction

Single-walled carbon nanotubes (SWNTs) have been expected for building blocks of nano-devices due to their small diameters and unique electrical properties. Recently, bio or gas sensors with field-effect transistors using SWNT channels were reported [1, 2]. In order to enhance their sensitivity, single-electron transistors (SETs) or single-hole transistors (SHTs) which operate at room temperature have been desired. Several SETs or SHTs using SWNT single-carrier islands have been reported because SWNTs are very suitable for single-carrier island due to their 1~2 nm diameters. However, many of them showed their SET or SHT characteristics at low temperature (<150 K) [3]. In order to realize room temperature operation, very low total capacitance (C_{Σ} $\sim 10^{-18}$ F) is needed. From the simple cylinder model $[C=2\pi\varepsilon_{\rm r}\varepsilon_0 L/\ln(2h/r)]$, where L and r is the length and diameter of SWNT channel, respectively, and h is the thickness of SiO₂], less than 50 nm island is necessary for room temperature operation. Such small islands are very difficult to fabricate even though conventional electron beam lithography technique is used. In this paper, we fabricated a SHT using nanometer-sized gap junctions by shadow evaporation method [4], and they showed room temperature SHT behaviors.

2. Fabrication process

SHTs were fabricated on thermally grown 100-nm-thick SiO₂ on n^+ -Si substrate. After 5-nm-thick cobalt catalyst layer was deposited, SWNT channels were grown by thermal chemical vapor deposition method at 820°C for 10 min. Ethanol was used as a carbon source. Then, 1-nm-thick aluminum layer was deposited and naturally oxidized at room temperature for 30 hours. This oxidized aluminum layer worked as enhanced tunnel barriers for the single-hole islands. Next, Source electrodes were formed by conventional photolithography and lift-off method. Although drain electrodes were defined by similar procedure, the substrate was angled as shown in Fig. 1 so that the drain electrode was partially shadowed by the source electrode during evaporation process. In this method, the electrode separation can be extremely small. Figure 2 shows the SEM image of the device. SWNT channel and approximately 20-nm-gap junction could be observed.

Current-voltage characteristics were measured by a semiconductor parameter analyzer B1500A (Agilent Technology Inc.) at 295 K.



Fig. 1 Schematic illustration of shadow evaporation.



500 nm

Fig. 2 SEM image of the nano gap junction formed by the shadow evaporation.

3. Results and discussion

Figure 3 shows the drain voltage dependence of the drain current for several gate voltages. The drain currents basically decreased with increasing gate voltage, which indicate that the carrier type of the device was positive. This p-type characteristic is considered to be due to adsorption of O_2 molecules.

The drain current versus gate voltage characteristic for several drain voltages at 295 K was shown in Fig. 4. The drain currents were clearly oscillated with increasing the gate voltage. This phenomenon is room temperature Coulomb oscillation. The peak and valley positions were almost the same for the different drain voltage.



Fig. 3 Drain current versus drain voltage characteristics for several gate voltages at 295 K.



Fig. 4 Gate voltage dependence of the drain current at 295 K.

Figure 5 shows contour plots of the drain current at 295 K as functions of the gate and drain voltages. Apparent Coulomb diamonds could be seen at room temperature. These phenomena indicate that single-hole island was successfully formed by nano gap junction on the SWNT channel.

3. Conclusions

Room-temperature operated SHT was successfully fabricated using SWNT. The 20 nm-nano-gap junction could be formed by the shadow evaporation. The device showed clear Coulomb oscillations and Coulomb diamonds at 295 K.



Fig. 5 Contour plots of the drain current as functions of the drain and gate voltages at 295 K.

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