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Recent Progress in "Beyond CMOS" Information Processing Technologies

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Moore's Law is the key engine that has driven the semiconductor industry over the past 40 years by providing more functions per chip at significantly lower cost per function. Intel sees this continuing for many years. However, CMOS scaling could reach limits based on physical limits of atomic structures or power density by around 2020 and will certainly become more costly and difficult in that time frame. To address this, Intel and the rest of the industry is looking beyond CMOS information processing technologies and considering the use of novel materials, computing mechanisms and logic devices.

Intel, in collaboration with universities and industrial research consortia, is investigating alternative information processing technologies such as spin torque memory, Ge spinFETs, spin wave logic, nonequilibrium systems, pseudospintronics, spin wave amplifiers, magnetoelectric and multiferroic materials and multiferroic MQCAs. Although no clear replacement for CMOS has been identified, solid, scientific progress is being made. As recently as 5 years ago, the search for alternative information processing technologies was in its infancy with only a few potentially interesting physical effects having been identified. In the intervening 5 years, solid device concepts have emerged, a few have been fabricated and characterized in proof of principle experiments and prototyping activities will start soon. Perhaps more importantly, progress in developing alternative technologies is no longer "idea limited" although new ideas will continue to emerge. Rather, it is limited by well understood issues such as material properties, fabrication and characterization that are common to making progress in more traditional technology research.

The role of international working groups such as International Technology Roadmap for Silicon (ITRS) and International Planning and Working Group for Nanoelectronics (IPGWN) has been indispensable to this process. The technology assessments and resulting roadmaps have greatly influenced the scope of regional research programs such as the Nanoelectronics Research Initiative (NRI) in the US, the European Nanoelectronics Initiative Advisory Council (ENIAC) and Advanced Institute of Science and Technology (AIST) in Japan. The NRI has already produced significant research highlights including the ones described briefly below.

Spin MOSFETs [1] configurations with ferromagnetic source / drain configurations have been analyzed and simulated. High spin injection and extraction efficiencies coupled with long spin decoherence lengths are required to achieve high magnetocurrent ratios substantially greater than 10^5. The NRI

is investigating spin MOSFETs with Co and Ni source drain contacts onto Ge channels based on related experiments show very low Shottky Barriers of 0.06 -0.08eV in related experiments.

In addition, logic circuits based entirely on magnetic information storage, manipulation, input and output [2] have been fabricated and tested. The information from distant devices is transmitted via a magnetic field encoded as spin waves propagating in a spin wave bus using room temperate NiFe and CoFe films. Experimental data demonstrating enhanced logic functionality based on nonvolitale logic devices is presented along with simulations that evaluate potential performance advantages and disadvantages relative to scaled CMOS.

The novel approach to non-equilibrium operation to achieve subthreshold I/V slopes significantly less that 65 mV /decade have been proposed[3] . It utilizes a ferroelectric material to produce a negative capacitance in series with the body capacitance that effectively acts as a voltage multiplier with factors as voltage multiplication as large as 4. Experimental verification is under way

Pseudospintronic dvices have been proposed [4] which consist of two graphene monolayers separated by a thin dielectric of approximately 1 nm. The device exploits an exchange-correlation (interaction) enhancement of the quasiparticle interlayer tunneling amplitude. Simulations predict a maximum on current of .3 mA with a 0.4 V supply and an extremely high Ion/Ioff ratio.

In parallel with development of new devices and device concepts, breakthrough work in novel materials and material heterostructures is taking place[5]. One example is the development of room temperature magnetoelectric materials such as BFO which allow direct control of magnetic polarization through an applied electric field. A related demonstration of a quantum exchange interaction across a heterojunction opens the door to a great many potential device concepts.

Intel believes that novel materials and devices integrated with advanced CMOS platforms and design concepts will extend the trajectory of Moore's Law through for many more generations.

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