Lateral Buried Growth of N⁺-InGaAs Source/Drain Region to Undercut InGaAs Channel Structure for High Drive Current N-type MOSFET

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1. Introduction

According to ITRS [1], III-V semiconductor device technology will potentially be introduced into LSI technology for realizing circuits with greater capabilities than current CMOS circuits. In fact, logic applications using III-V devices have already been researched [2]–[4]. In previous researches, conventional InP-based transistors were fabricated as HEMT device structures [2]–[4]. However, a selective strongly doped source and drain (S/D) region is required in order to achieve high current density and low access resistance between the source and the channel with an enhancement mode [5,6]. However, ion implantation technology in InP-based materials is not yet sufficiently advanced. Thus, regrowth technology is a promising alternative technique. Furthermore, a slight overlap between the gate electrode and source is also necessary to improve the average velocity of electrons at the source end of the channel. Regrowth source regions have to penetrate under the gate electrodes. We have reported the lateral buried growth of n⁺-InGaAs in order to build a contact with a quantum well channel under the SiO₂ dummy gate and regrown source region.

2. Design and Experiment

Figure 1 shows a schematic cross-sectional image of the MOS structures proposed in this research. The channel layer comprises a 12-nm-thick InGaAs layer that is lattice matched to InP substrates and is expected to have high electron mobility [7]. The channel is sandwiched by AlInAs layers since barrier and carrier electrons will be confined in the quantum well structure. The top AlInAs layer must be as thin as possible to obtain a large inversion-layer capacitance.

![Figure 1 Schematic image of the proposed MOSFET structure](image)

In this research, we aim to achieve a drive (drain) current density of 3 mA/μm. In order to achieve the estimated value, the Fermi energy in the source region must be approximately 0.3 eV for a carrier concentration of $9 \times 10^{12} \text{ cm}^{-2}$ (6 $\times 10^{12} \text{ cm}^{-2}$ in the first state and 3 $\times 10^{12} \text{ cm}^{-2}$ in the second state) taking the electron velocity into account. The Fermi energy is lower than both the conduction band discontinuity at the heterointerface between AlInAs and InGaAs and the L-band energy in the InGaAs channel. Thus, carriers are confined in the channel layers and a large inversion-layer capacitance is maintained in a small effective mass $m^*$ (such as InGaAs $m^* = 0.04$). However, a thin AlInAs barrier is not adequate to suppress the gate leakage current. Therefore, an insulating layer such as HfO₂ or Si₃N₄ must be used between the gate electrode and AlInAs. The doping concentration of the regrowth layer is made as high as possible to supply a sufficient number of carriers to the channel and as low as possible to shut the injection into the AlInAs barrier layers or L-band. The requirements are achieved at a doping concentration of $1 \times 10^{19} \text{ cm}^{-3}$, which is reasonable in conventional crystal growth techniques. However, the surface region separated channel should be doped at $3 \times 10^{19} \text{ cm}^{-3}$ [8] in order to reduce the contact resistance with the electrode metals.

First, in order to establish fabrication techniques for the above-mentioned device, we focused on the growth technique of the S/D region and performed experiments as follows. Figure 2 shows a schematic image of the samples used for regrowth examinations. The fabrication process is as follows. First, a 60-nm-thick SiO₂ layer was deposited by the plasma CVD method. Then, a 1-μm-wide line and space pattern was fabricated by CF₄ dry etching. Next, the InP cap layer and upper AlInAs layer were removed by wet etching by a HCl:H₂O = 3:1 solution for 5 s.

![Figure 2 Schematic image of regrowth sample structure](image)
Then, the InGaAs channel was selectively wet etched by a solution of citric acid:H₂O₂ = 1:1 for 30 or 60 s at RT. The selectively etched substrates were immediately loaded into a MOVPE chamber and n⁺-InGaAs with a donor concentration of 1 × 10¹⁹ cm⁻³ was grown at 570 °C.

3. Result and Discussion

For a selective etching time of 60 s, the InGaAs channel undercut length was approximately 80 nm, as shown in Figure 3 (a). After MOVPE growth, n⁺-InGaAs was extended into the quantum well structure. However, the grown InGaAs was not connected with the channel. The maximum length of the buried region was approximately 50 nm, while that of the space was nearly 30 nm (as shown in Figure 3 (b)). This phenomenon occurred because the migration length was too short as compared to the undercut length. Then, the grown n⁺-InGaAs region was stacked at the entrance of the undercut region, and the source region could not be connected with the quantum well channel.

In the case of a selective etching time of 30 s, Figure 3 (c) shows that the length of the undercut was approximately 40 nm. After MOVPE growth (in Figure 3 (d)), the undercut region was filled by the InGaAs. The lateral buried growth length of InGaAs was approximately 40 nm under the growth condition in this experiment. The observed length is sufficient to form an overlap in proposed device.

4. Conclusions

We have demonstrated the lateral buried growth of n⁺-InGaAs into the undercut region in the InGaAs quantum well channel structure for a high drive current MOSFET. A lateral growth of over 40 nm was clearly observed for a 12-nm-thick InGaAs thin film layer sandwiched by AlInAs. The buried length of the grown layer was sufficient to connect the grown source with the channel as compared to the case of the gate and sidewall structures in the self-aligned nanoscale FETs. The result indicates the possibility of realizing a 3-mA/µm current density in future VLSI integrated III-V self-aligned MOSFET structures.

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References

[1] ITRS 2007 PIDS, p. 33