Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 310-311

G-3-3

40 Gbit/s Operation of MOBILE Using Only RTDs and Its Application to 2-bit Flash ADC

Hyungtae Kim, Kangil Lee, Yunho Kim, and Kwangseok Seo

Seoul National Univ., School Of Electrical Engineering and Computer Science
San 56-1, Shillim-dong, Kwanak-ku, Seoul 151-744, Korea
Phone: +82-2-877-0298 E-mail: kht086@snu.ac.kr

1. Introduction

Resonant tunneling diode (RTD) is one of the most promising candidates for future nanoelectronics devices [1]. RTD circuits have been widely studied for their ability in achieving high speed operation, high functionality with reduced circuit complexity, and low power consumption owing to their ultra high-speed switching characteristics and negative differential resistance (NDR) features. Various high-speed and low-power logic applications based on Monostable-to-Bistable Transition Logic Element (MOBILE) have already been demonstrated [2], [3].

However, in the previously reported MOBILE-based circuits, the transistors, which were used to modulate the peak current, have limited the full exploitation of the high-speed switching and low-power features of RTDs [4]. For example, MOBILE operation was demonstrated only up to 35 Gbit/s with about 2 mW power dissipation in spite of picoseconds level switching time of RTD [2]. Logic circuits using only RTDs in the 1960's [5] can be used to overcome these limits. For example, as an attempt to solve this problem, various logic circuits using only RTDs were proposed recently [4], [6]-[8]. Motivated by the previous results, we have proposed and demonstrated MOBILE circuits and multi-valued logic (MVL) circuits using only RTDs as active devices [9], [10]. In this paper, we report 40 Gbit/s operation of MOBILE using only RTDs, and its application to 2-bit flash analog-to-digital-converter (ADC).

2. Circuit Configuration

Fig. 1(a) shows the circuit configuration of MOBILE using only RTDs. MOBILE is a rising edge triggered logic element which consists of two series-connected NDR devices. The circuit configuration of the proposed MOBILE is the same as that of the conventional MOBILE except for the input-driver as shown in Fig. 1(a). The proposed MOBILE consists of a series-connected RTD pair and a RTD-resistor pair for monostable-to-bistable transition and current modulation, respectively, as shown in Fig. 1(a). The detailed operation principles of the proposed MOBILE using only RTDs have previously been reported [9].

By implementing an RTD-resistor pair at the input stage, multi-valued logic circuit can be implemented with reduced circuit complexity. We have demonstrated MVL operation using the same circuit configuration with MOBILE with reduced circuit complexity compared with that of the previously reported MVL circuits [10]. To demonstrate the possibility of practical application of the proposed circuit configuration using only RTDs as active devices, we designed 2-bit flash ADC circuit using the proposed literal gates. Fig. 1(b) shows the circuit configuration of the designed 2-bit flash ADC using only RTDs. Up-literal operation is used for MSB signal generation, and literal operation with two thresholds is used for LSB signal generation to generate 2-bit Gray-coded output signal. The proposed ADC uses only 8 devices (6 RTDs and 2 resistors). The device count is drastically reduced compared with that of the previously reported RTD-based 2-bit flash ADC, which uses 26 devices [11].

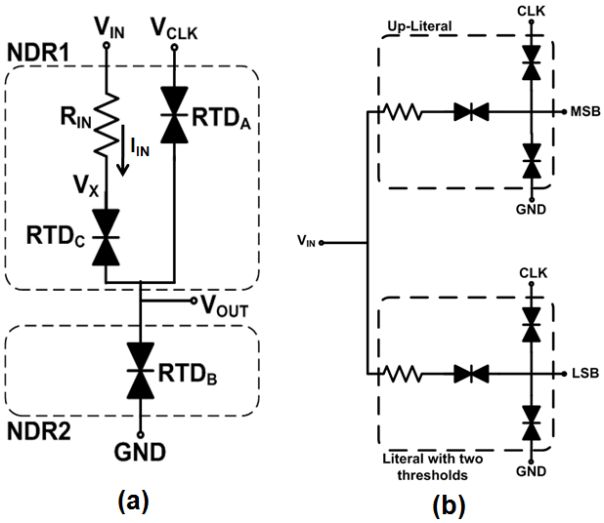

Figure 1. (a) Circuit configuration of MOBILE using only RTDs. Series connected RTD pair (RTD_A and RTD_B) is used for monostable-to-bistable transition, and RTD-resistor pair (RTD_C and R_{IN}) is used for peak current modulation. (b) Circuit configuration of 2-bit flash ADC using only RTDs. Utilizing nonlinear foldback I-V characteristics of RTD, MSB and LSB signal can be implemented using the same circuit configuration with that of the MOBILE.

3. Fabrication and Measurement Result

Test circuits were fabricated using our RTD technology on an InP substrate. AlAs/InGaAs/InAs RTD epitaxial layers were grown by MBE. To fabricate designed ICs, the conventional optical lithography and the lift-off process were used. The peak current density of the fabricated RTDs was 112 kA/cm^2 with a good peak-to-valley current ratio of 12 at room temperature, and the peak voltage of the fabricated RTDs was about 0.3 V. Fig. 2(a) shows the microphotograph of the fabricated MOBILE using only RTDs. To minimize measurement system effect, we included input/clock buffers in the test circuit. We used simple 50 ohm resistor for input and clock buffers. Simple 400 ohm resistor was used for output buffer. Fig. 2(b) shows the measurement result at 40 Gbit/s with an input bit pattern of

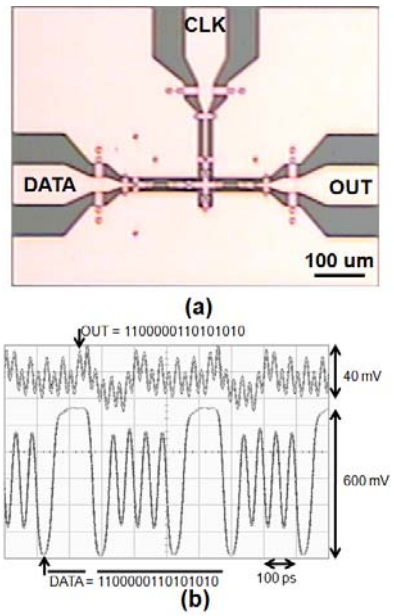

Figure 2. (a) Microphotograph of the fabricated MOBILE circuit. (b) Measured input/output bitstream of the fabricated MOBILE circuit at 40 Gbit/s.

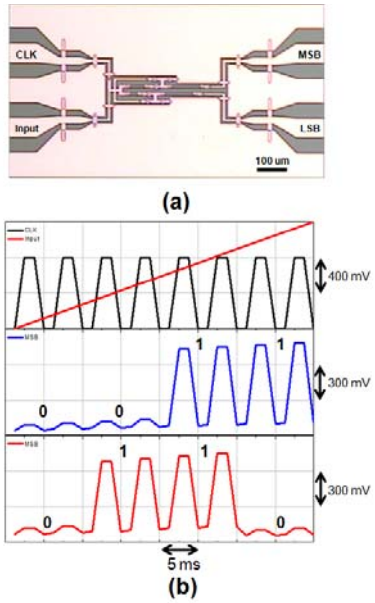

Figure 3. (a) Microphotograph of the fabricated 2-bit flash ADC. (b) Measurement result of the fabricated 2-bit flash ADC at a clock signal of 200 kHz and an input signal of 25 kHz.

(1100000110101010). The lower trace is the complement of the input data stream. The upper trace shows the output waveform. As shown in this figure, the logic function of the fabricated MOBILE as a noninverted return-to-zero-mode delayed flip-flop with about 40 mV output swing has been confirmed at 40 Gbit/s. The output swing is relatively small because simple 400 ohm resistor is used as an output buffer. The estimated power dissipation was about 1.2 mW at 40 Gbit/s.

Fig. 3(a) shows the microphotograph of the fabricated 2-bit flash ADC using only RTDs. Fig. 3(b) shows the measurement result of the fabricated 2-bit flash ADC. As shown in Fig. 3(b), 2-bit Gray code output was successfully obtained at a clock signal of 200 kHz and an input signal of 25 kHz. The operation of the fabricated ADC was confirmed at low frequency, but we can expect high frequency operation from the 40 Gbit/s operation of the MOBILE with the same circuit configuration.

4. Conclusion

In summary, we have demonstrated 40 Gbit/s operation of MOBILE with very low power dissipation of about 1.2 mW using only RTDs. The power dissipation can be more reduced using scaled down devices. The proposed circuit configuration has advantage that MVL circuits can be implemented using drastically reduced circuit complexity compared with that of the previously reported circuits. To demonstrate the potential of the proposed circuit configuration using only RTDs for MVL logic applications, we have also designed and fabricated 2-bit flash ADC with reduced circuit complexity compared with that of the previously reported RTD-based ADCs. These results indicate the great potential of the proposed circuits using only RTDs for future nanoelectronic logic applications.

Acknowledgements

This work was financially supported by the National program for Tera Level Nano Devices of the Ministry of Science and Technology as one of the 21st Century Frontier programs. The authors would like to thank S. Choi and Professor K. Yang of KAIST for their assistance in measuring the fabricated circuit.

References

[1] International Technology Roadmap for Semiconductors, 2005 version.
[2] K. Maezawa, H. Matsuzaki, M. Yamamoto, and T. Otsuji, “High-Speed and Low-Power Operation of a Resonant Tunneling Logic Gate MOBILE”, IEEE Electron Device Lett. Vol. 19, pp. 80~82, 1998.
[3] K. Maezawa, “Resonant tunneling diodes and their application to high-speed circuits”, in Proc. IEEE Compound Semiconductor Integrated Circuit Symposium, pp. 97~100, 2005.
[4] T. Waho, A. Yamada, H. Okuyama, V. Khorenko, T. Do, and W. Prost, “A Four-Resonant-Tunneling-Diode (4RTD) NAND/NOR Logic Gate”, in Proc. IEEE International Symposium on Circuits and Systems, pp. 129~132, 2007.
[5] R. C. Sims, E. R. Beck. Jr., and V. C. Kamm, “A survey of Tunnel-Diode Digital Techniques”, Proc. IRE. vol. 47, pp. 1304~1316, 1961.
[6] William Williamson, III, Steven B. Enquist, David H. Chow, Howard L. Dunlap,Suresh Subramaniam, Peiming Lei, Gary H. Bernstein, and Barry K. Gilbert, “12 GHz Clocked Operation of Ultralow Power Interband Resonant Tunneling Diode Pipelined Logic Gates”, IEEE J. Solid-state Circuits, vol. 32, pp. 222~231, 1997.
[7] T. Tanaka, Y. Ohno, S. Kishimoto, K. Maezawa, and T. Mizutani, “Experimental Demonstration of Capacitor-Coupled Resonant Tunneling Logic Gates for Ultra-short Gate-delay Operation”, Jpn. J. Appl. Phys., vol. 42, pp. 6766~6771, 2003.
[8] K. Maezawa, H. Sugiyama, S. Kishimoto, and T. Mizutani, “100 GHz Operation of a Resonant Tunneling Logic Gate MOBILE Having a Symmetric Configuration”, in Proc. IEEE International Conference on Indium Phosphide Related Materials, pp. 46~49, 2006.
[9] H. Kim and K. Seo, “Noninverted/Inverted Monostabel-to-Bistable Transition Logic Element Circuits Using Three Resonant Tunneling Diodes and Their Application to a Static Binary Frequency Divider”, Jpn. J. Appl. Phys., vol. 47, pp. 2854~2857, 2008.
[10] H. Kim and K. Seo, “MOBILE-based Literal Gates Using Resonant Tunneling Diodes”, Jpn. J. Appl. Phys., to be published.
[11] T. Itoh, T. Waho, J. Osaka, H. Yokoyama, and M. Yamamoto, “Ultrafast analog-to-digital converter using resonant-tunneling ternary quantizers”, in Int. Microwave Symposium Digest, pp.197-200, 1998.