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Failure Mechanisms of GaN-Based Transistors in On-and Off- State

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1. Introduction

GaN HEMTs are extremely promising for power electronics applications from power conditioning to microwave amplifiers and transmitters [1]. Front-end applications are also interesting, due to the intrinsic robustness and survivability of high breakdown voltage GaN HEMTs, coupled with reasonable noise figures. Satellite communications, high performance radars and commercial ground base stations currently represent target system applications.
Due to their high breakdown voltages, GaN devices can operate in conditions that are not readily realizable with other device technologies [2], i.e. high drain operating voltage, low output capacitance per unit power (resulting from high power density), high peak efficiency, and good thermal dissipation.
Record device performances (NOT simultaneously achieved) include extremely high output power (900W @2.9 GHz, 81 W @9.5 GHz), high frequency f_T = 181 GHz @ L_g=30 nm, high power efficiency PAE = 75% @P_{sat}= 100 W, broad band operation 1.0 - 2.5 GHz with 50% efficiency [3].

Nowadays GaN HEMTs devices with record performances were realized: power densities as high as 20 to 40 W/mm [4], [5] and absolute powers up to 500W [6]. A number of demonstrations of GaN-based Doherty amplifiers were achieved, e.g. [7,8] for increasing the efficiency in linear operation. Class-E amplifiers based on GaN HFETs with PAE levels beyond 80% and 10 W of output power at 2 GHz have been reported [9]. Switch-mode class-F amplifiers based on GaN HFETs are also very promising [10].

Achieving a high level of reliability and stability concurrently with high-performance operation may remain a challenge, due to the peculiarities of the physics of Gallium Nitride devices, to material imperfection, to the sensitivity of technology to processing conditions [11]. This paper will review failure modes and mechanisms of GaN HEMTs and will propose a methodology for the evaluation of their reliability, based on the experience accumulated at the Microelectronics Laboratory of the University of Padova, in collaboration with several industrial laboratories in Europe and elsewhere [12].

3. Reliability evaluation of GaN HEMTs

In general, reliability of GaN-based High Electron Mobility Transistors is affected both by *"intrinsic"* failure mechanisms related to the high voltage and high electric field operation of these devices (like hot-electron-induced degradation [13], or defect generation due to the inverse piezoelectric effects [14]) and *"extrinsic"* degradation effects, which are related to the defectivity of the materials, or the damage introduced by specific process steps. Even if thermal stability of Schottky and ohmic contacts and of passivation may represent an issue due to the relatively high operating temperatures and heavy thermal cycling of these devices, very frequently the observed failure modes observed after DC accelerated testing at high V_{DS} involve generation of deep levels and trap-related degradation mechanisms. A full evaluation of these mechanisms therefore requires: (a) a characterization of hot-carrier effects, capable of identifying which are the most dangerous bias points for device operation, to evaluate the amount of stress imposed during accelerated test, to identify the presence of hot carriers within the devices, and to compare different device structures from the point of view of internal electric fields and of hot carrier phenomena; (b) diagnostic techniques suitable for the evaluation of deep levels and defects generation.
In GaAs devices, hot carrier effects are usually evaluated by measuring the gate current due to collection of holes generated by impact ionization [15]. Unfortunately, in GaN HEMT's impact ionization is negligible, and the gate current is dominated by tunneling injection mechanisms and can not be used as an indicator of hot-electron phenomena. We demonstrated in [12],[16] that electroluminescence microscopy and spectroscopy [17] can be a good indicator of hot-electron concentration in GaN HEMT's, thus allowing one to identify appropriate testing conditions for studying those effects.

Since deep levels generation is the most common degradation mechanism during tests at high V_{DS} or V_{DG}, suitable diagnostic techniques must be adopted; these include double-pulse gate-lag measurements, enabling the measurements of pulsed I_D vs V_{DS} characteristics starting from an arbitrary V_{DS}, V_{GS} baseline point; since electron trapping usually occurs in pinch-off conditions, transient effects are enhanced by using higher V_{GD} baseline values, thus increasing the sensitivity of the technique to trapping effects. When the channel is opened, electrons can not be released or compensated immediately, and the consequent slow response of drain current induces the "current collapse" effect. Trap-related issues can be quantitatively evaluated using current Deep Level Transient Spectroscopy, while transconductance dispersion measurements as a function of frequency can provide information concerning the effect of traps on the device small-signal linearity.

Hot-electron degradation

Several authors have observed parametric and gradual degradations of GaN HEMTs (decrease in I_{DSS} and g_m, increase in gate-lag effects) which were not accelerated by the electric field *only* (maximum degradation close to pinch-off conditions), but required both channel current *and* high electric fields, thus involving the presence of hot electrons. Hot electrons can be trapped on the device surface, in the AlGaN or in the buffer, giving rise to reversible degradation of I_{DSS} and g_m; they can also generate traps (thus increasing current collapse and gate-lag effects), thus promoting further charge trapping.

Several features reported in the literature tend to confirm this hypothesis:

(a) degradation involves the surface of the AlGaN: [18];

(b) passivation of the device surface with SiN has a healthy effect on hot-electron degradation; [18],[19]; reliability is improved if a low-power NH_3 plasma treatment is adopted before depositing the SiN passivation layer [20], [21] possibly through the incorporation of hydrogen which would passivate traps.

(c) Jha et al. [22] have studied the influence of gate recess depth, formed by reactive ion etching, on hot-electron degradation in GaN HEMT's; they concluded that a drastic increase in the interface trap density at the AlGaN/GaN heterointerface resulted from the hot electron stressing experiment. Another mechanism induces an early degradation of I_{DSS}: the larger the recess, the faster the degradation.

(d) Noise measurements were adopted by Valizadeh and Pavlidis in order to study the effect of DC and rf stress on AlGaN/GaN HEMT's [23]: they concluded that hot electron trapping is responsible for the observed degradation in both DC and rf tests.

(e) Coffie et al. [24] observed a negative activation energy for the degradation of output power in the junction temperature range -55°C to 205°C and concluded that hot carrier induced degradation is the dominant degradation mechanism. However, there is no agreement on this topic in the literature, and that many authors have reported thermally-activated degradation of GaN HEMT's, with positive activation energies ≈ 1.05 - 2.0 eV

Inverse piezoelectric effect and materials related issues

A new mechanism has been recently proposed by Joh and del Alamo [14]: the electric field in the gate-drain region would increase the strain in the AlGaN/GaN heterojunction ("inverse piezoelectric effect") eventually resulting in strain relaxation and crystallographic defect formation. This would compromise carrier transport properties and electron concentration in the access region, thus increasing R_D and reducing g_m; gate leakage current would then increase due to the enhanced trap-assisted tunneling and hopping phenomena in the AlGaN. This failure mechanism would be thermally-activated with a positive activation energy (which is inconsistent with the channel hot-electron degradation mechanism), which has been actually observed by many authors. Joh and del Alamo have found that there is a critical gate-drain voltage which triggers this effect, around $V_{GD} \approx$ 20-30 V for the tested devices [14].

In other cases, a dependence of GaN HEMT reliability on epitaxial material quality was found [25]; off-state testing of GaN devices was found to induce localized defects, possibly related with the pre-existing defect density in the material, detected by EL or IR microscopy [16],[26]

Conclusions

Most dangerous failure mechanisms of GaN HEMTs appear to involve trap generation, either due to hot electron degradation, reverse piezoelectric effects, or localized damage due to trap-asssisted current injection. Specific diagnostic techniques may assist reliability studies providing useful hints for device and material optimization.

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