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Electrical properties of 4H-SiC CMOS with wet processed gate oxide

Mitsuo Okamoto, Tsutomu Yatsuo, Kenji Fukuda, and Hajime Okumura
Energy Semiconductor Electronics Research Laboratory (ESERL), Advanced Industrial Science and Technology (AIST)
Tsukuba central 2, 1-1-1 Umezono, Tsukuba, Ibaraki 305-8568, JAPAN
E-mail: mitsuo-okamoto@aist.go.jp

Silicon carbide (SiC) is an attractive material for high-power and high-temperature devices because of its superior properties. SiO_2 layer can be grown on the SiC by means of thermal oxidation and a number of discrete low-loss and high-power SiC MOSFETs have been demonstrated to date. It is also another advantage that those SiC devices can operate at high temperature such as 300 ºC, but Si-based system drive circuits cannot be used at such high temperature. SiC integrated circuits (ICs) composed of SiC power MOSFETs and SiC CMOS will realize high-temperature power module.

We have reported that the wet oxidation could provide the relatively high channel mobility (15.6 cm^2/Vs) and low threshold voltage for Si-face 4H-SiC p-channel MOSFETs (pMOS) [1]. In this study, we attempted to fabricate 4H-SiC CMOS utilizing those techniques. The channel mobility for 4H-SiC nMOS, however, became quite poor (~1 cm^2/Vs) by the wet gate oxidation (pyrogenic wet oxidation at 1200 ºC). We employed buried-channel (BC) structure in order to improve the properties of SiC nMOS. We investigated the effects of BC structure on 4H-SiC nMOS before fabrication of SiC CMOS. The BC-nMOS was fabricated on the p-well region formed on the n-type epitaxial SiC layer by one-shot aluminum ion implantation (400keV) with the total dose of $2x10^{13}$ cm^{-2}. BC structure was formed by ion implantation of nitrogen with box profile at depth of 0.15 µm. The electrical properties of BC-nMOS depended drastically on the concentration of the BC-layer, as shown in Fig. 1. We could obtain the BC-nMOS with the channel mobility of 63.9 cm^2/Vs and the threshold voltage of 1.3 V.

We also fabricated SiC CMOS utilizing those results. Fig. 2 shows the schematic figure of SiC CMOS fabricated in this study. SiC CMOS was fabricated on n-type epitaxial layer grown on Si-face n-type 4H-SiC wafer. PMOS was fabricated on the n-type epitaxial layer, and nMOS was fabricated on p-well region. The channel length (L_{ch}) of SiC CMOS was 2 µm. The typical channel width (W_{ch}) was 20 µm for nMOS and 80 µm for pMOS, respectively.

The inverter transfer characteristics of SiC CMOS at supply voltage of 10 V are shown in Fig. 3. The inverter voltage transfer characteristics were stable up to 300 ºC. Ring oscillators were also fabricated to determine the operation speed. Fig. 4 is the output waveform for 81-stage ring oscillators comprised of serially cascaded inverters at supply voltage of 15 V. The delay time per stage of the ring oscillator was calculated as 40.0 ns at room temperature.

[1] M. Okamoto, M. Tanaka, T. Yatsuo and K. Fukuda: Appl. Phys. Lett. Vol. 89 (2006), p. 023502-1

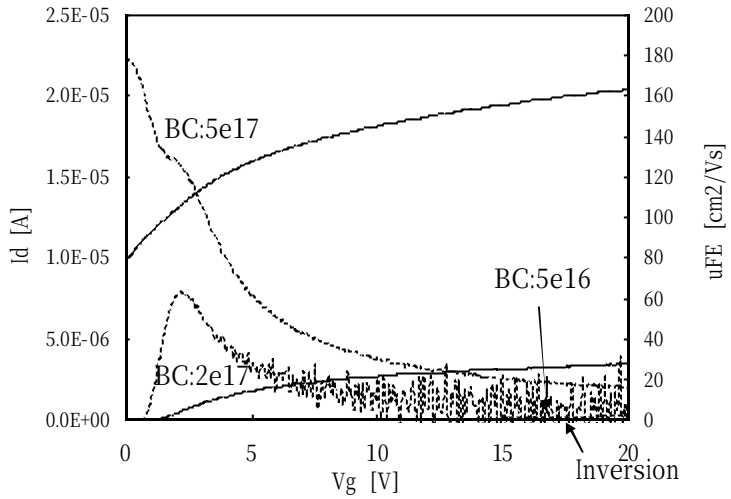

Fig. 1. I_d-V_g and μ_{FE}-V_g characteristics for buried-channel nMOS with various concentration of BC-layer. Solid line and dashed line represent I_d-V_g and μ_{FE}-V_g curve respectively. The electrical properties for BC-nMOS depended drastically on the concentration of the BC-layer.

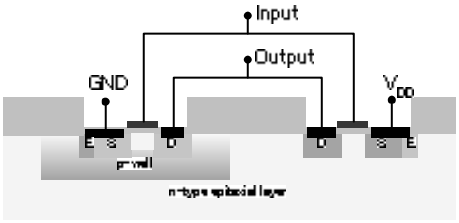

Fig. 2. Schematic figure of 4H-SiC CMOS fabricated in this study.

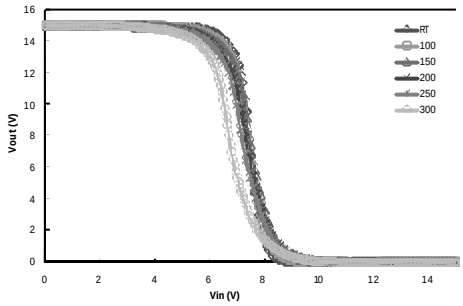

Fig. 3. 4H-SiC CMOS inverter voltage transfer characteristics. Stable inverter operation could be observed up to the temperature of 300 ºC.

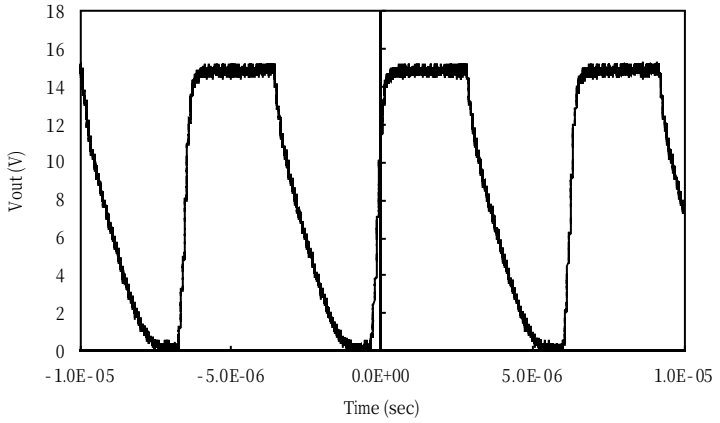

Fig. 4. Output waveform for 81-stage ring oscillators comprised of serially cascaded inverters at supply voltage of 15 V. The delay time per inverter stage was calculated to be 40.0 ns.