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Threshold Voltage Shift in Ga_2O_3-In_2O_3-ZnO (GIZO) Thin Film Transistors under Constant Voltage Stress

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1. Introduction

In recent years, oxide semiconductors[1,2] attract much attention as promising material for driving thin film transistors of new display(Fig.1). Features of this material are low fabrication temperature lower than 200℃, considerably high electric properties compared with amorphous silicon TFTs. High performance enables us to design the peripheral circuit. Furthermore, owing to their wide band gap, they are regarded as materials for "transparent electronics".

Reliability is one of the serious problems for realization of the new display using oxide semiconductors. However, there has been no paper analyzing the degradation systematically under circuit operation[3,4].

In this study, we evaluated the reliability of oxide semiconductor TFT with amorphous Ga_2O_3-In_2O_3-ZnO (GIZO)[5] by applying gate and drain voltage stress. We discussed the degradation by drain voltage and/or current flow assuming circuit operation. Thermal imaging system[4] was used to analyze thermal distribution during the stress.

2. Experimental

Schematic cross sectional image of GIZO thin film transistor[5] is shown in Figure 2 After the patterning of gate metal, SiN film with a thickness of 400nm was deposited by PECVD at 300℃ as gate insulator. Then GIZO film with a thickness of 70 nm was deposited in mixed gas of Ar and oxygen. After the patterning of active layer, source and drain electrodes was formed by lift-off process. In_2O_3-ZnO source/drain was fabricated by rf sputtering.

For several gate size, various gate and drain voltages were applied as electric stress and the change of electrical properties were examined to evaluate the reliability. To analyze the degradation mechanism, thermal analysis using thermal imaging system (Infra scope II) was performed. In order to measure the recovery properties, change of the transfer curve was examined just after removing the stress.

3. Results and Discussion

Threshold voltage shift by gate voltage

Figure 3(a) show the change of transfer characteristics by gate voltage stress of 20V. With a passage of time, transfer curve and peak mobility shifted parallel to positive direction. Marked change in S parameter and mobility was not observed. Parallel shift without mobility change suggested the generation of electron traps without causing interface state generation.

Recovery Properties

Figure 3(b) shows the recovery properties after the stress imposition. After the imposition of gate voltage stress of 20V, recovery properties were measured without any stress at room temperature. Just after turning off the stress, transfer curves were recovered gradually with the passage of time. For the recovery time of 10000 sec, transfer curves almost recovered to initial level. This phenomenon is not observed in polycrystalline silicon or amorphous silicon. Thermal annealing was required for these TFTs to recover[6].

Degradation by Drain Voltage Stress

From above, we discussed the degradation by only gate voltage stress. Here, we investigated the effect by drain bias. To study the degradation of the TFT under operation in the peripheral circuits, effect by the drain bias is very important. Figure 4 shows the change of the transfer curve under the stress of gate and drain voltage Vg=Vd=20V. The shift of the transfer curve was similar to the case of gate only stress shown in Fig.3(a), parallel shift was observed with a passage of time. This similar change suggested that the degradation mode was not changed by the addition of drain voltage stress.

Imposition of drain voltage stress made us worry about the damage of Joule heating. We have previously reported that the Joule heating by drain current causes serious problems in the reliability in silicon TFT[4]. Hence, we investigated thermal distribution of the TFT.

Fig.1 Flexible AM-OLED driven by IGZO-TFTs (Ref. [7])

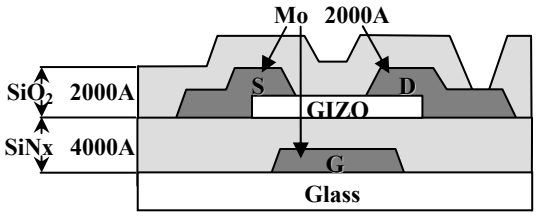

Fig.2 Cross sectional image of the Ga_2O_3-In_2O_3-ZnO (GIZO) thin film transistor.

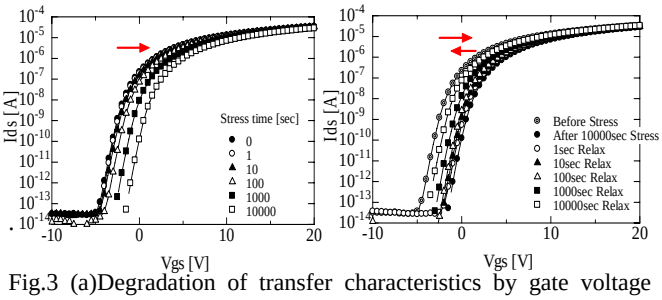

Fig.3 (a)Degradation of transfer characteristics by gate voltage stress of 20V. (b) Recovery properties after the stress imposition of 20V gate voltage stress.

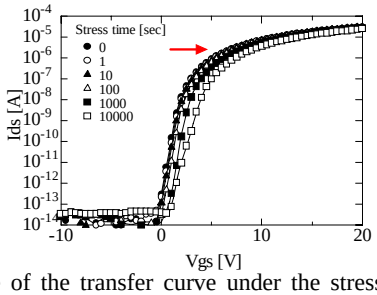

Fig.4 Change of the transfer curve under the stress of gate and drain voltage Vg=Vd=20V.

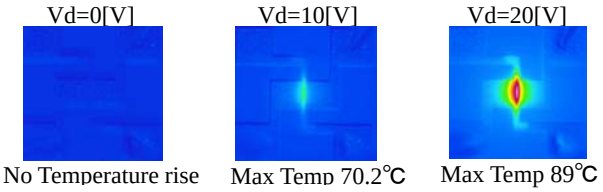

Fig.5 Thermal images obtained by thermal infrared imaging system (Infra scope II). Vg=20V and various drain voltage was applied. Gate size were W/L=150/8 μm. (Substrate Temp=60℃)

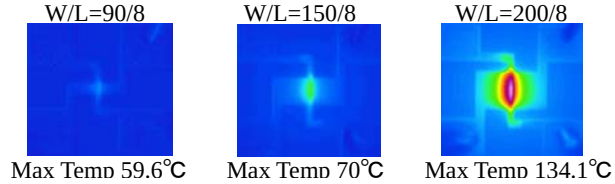

Fig.6 Thermal analysis of the TFT with various gate widths. Vd=Vg=20V was imposed. (Substrate Temp=60℃)

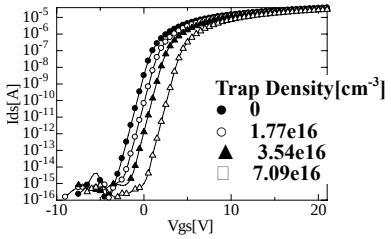

Fig.7 Simulation of parallel threshold voltage shift

Analysis of thermal distribution

Figure 5 shows the thermal images obtained by thermal infrared imaging system (Infra scope II). This figure shows the thermal distribution of TFT under various drain voltage with fixed gate voltage of 20V. This is the first report of the thermal image of oxide semiconductor TFT. For the drain bias of 0V, no thermal distribution was observed. With increasing drain voltage, temperature increased. For the drain voltage of 20V, temperature increased around 90℃ was observed. These drain voltage dependences suggested temperature increase were caused by Joule heating by drain current.

Thermal analysis of the TFT with various gate widths was performed as shown in Figure 6 Marked increase of the maximum temperature was observed with increasing gate widths. In the TFT with gate width of 200μm, maximum temperature of 130℃ was observed. By the increase of gate width, heat dissipation will be insufficient. Therefore, maximum temperature was increased in wide gate.

From the analysis shown in Fig.5 and 6, marked increase of the temperature by drain voltage and gate width was observed. However, we found that Joule heating does not accelerate the degradation observed in this TFT.

Degradation mechanism

In this study, unique degradation mode was observed in the GIZO TFTs. The features of this degradation are parallel threshold voltage shift depending on the gate voltage. Shifts exhibited logarithmic time dependent change. For the drain voltage stress, degradation mode was not affected; therefore, main cause was vertical electric field. This degradation was quite different from that by hot carrier effect observed in silicon TFTs[3].

Recovery properties without any thermal annealing suggest that very low energy is needed for the detrapping of the trapped carriers. Here, we propose shallow trapping state the interface between SiN and GIZO. To demonstrate this model, we performed the device simulation employing shallow trap states. In the vicinity of valence band edge, accepter-type trap were introduced in the model. As shown in Figure 7, degradation was reproduced. By increasing the trap density, threshold voltage shift without any change in S parameter was confirmed. The agreement between experiment and simulation demonstrated the validity of the model.

4. Summery

Degradation of GIZO thin film transistors was studied. We found a degradation mode which parallel shift without any change in transfer curve was observed. We confirmed that the mode was mainly dominated by vertical electric field. Marked acceleration of degradation by drain bias stress was not found. Thermal analysis was performed for the analysis of degradation mechanism. Temperature increase by drain voltage or gate sizes were observed, however, Joule heating did not accelerate the degradation. Recovery properties independent of the stress bias condition was observed. Degradation model employing shallow trapping states was proposed and its validity was demonstrated by the device simulation.

References

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