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Transparent Oxide Semiconductor-Based Self-Alignment Thin-Film Transistor

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1. Introduction

Recently, study on a thin film transistor (TFT) using an oxide semiconductor is actively carried out and SnO_2[1], ZnO_2[2], In-Ga-Zn-O (IGZO)[3] and In-Zn-O (IZO)[4,5] are used as a semiconductor. Especially, the IZO TFT was reported under low temperature annealing at 300℃ to decrease the carrier density due to an oxygen vacancy.[6] In addition, a transparent TFT using the transparent semiconductor was realized. With a further decrease of the annealing temperature, a fabrication of the TFT on a flexible substrate will be expected. In this study, we have investigated a self-alignment (SA)-IZO TFT using the IZO as the semiconductor, where gate insulator/ semiconductor interface is continuously deposited and back-surface exposure was done through transparent semiconductor.

2. Fabrication Process of Self-Alignment IZO TFT

Figure 1 shows a fabrication process of SA-IZO TFT. Glass substrate used was a fusion-formed aluminosilicate glass (Corning 1737). First, gate electrode of Ta (500 Å) was deposited and patterned using reactive-ion-etching (RIE) apparatus. After patterning the contact hole for lift-off, gate insulator of Ta_2O_5 (1,500 Å) and semiconductor layer of IZO (200 Å) were sequentially sputtered without breaking vacuum. Second, lift-off process of insulator/ semiconductor was carried out. And IZO film was patterned using an oxalic acid. Then, IZO film was annealed at 300℃ for 1h in air. Third, back-surface exposure was carried out, where the gate electrode was used as photomask. Where, semiconductor layer of IZO was transparent. This is remarkable point compared to a non-transparent amorphous silicon TFT[7] and an organic TFT.[8] In this top-contact type IZO TFT, continuous deposition of insulator and semiconductor can be carried out because the semiconductor layer was transparent. Fourth, an ohmic electrode of Cr (50 Å) / Au (500 Å) was evaporated and the lift-off process was carried out. After lift-off process, overlapping length between gate/ source and gate/ drain electrodes was as small as 0.5 μm. Fifth, patterning and etching of the ohmic electrode was done using aqua regia and cerium (IV) diammonium nitride solution. And then, interconnection of Cr (50 Å)/ Al (2,000 Å) was formed using lift-off technique. Finally, second annealing was carried out at 300℃ for 1 h in air. Etching condition of the gate electrode was as follows: flow rate of CF_4 of 10 sccm and gas pressure of 3.8 mTorr. A manual prober (Micronics 705A-6) and a parameter analyzer (HP 4155B) were used to measure electrical characteristics.

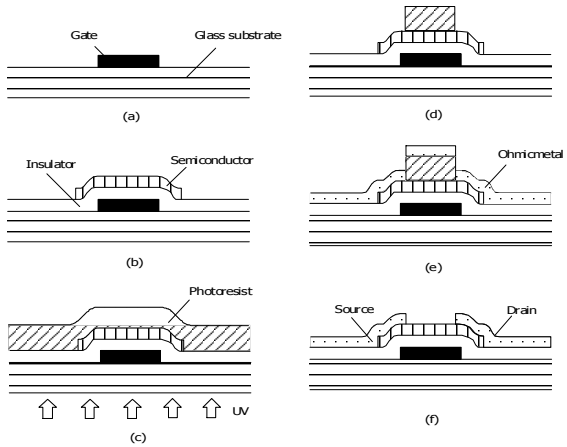

Fig. 1 Fabrication process of SA-IZO TFT.

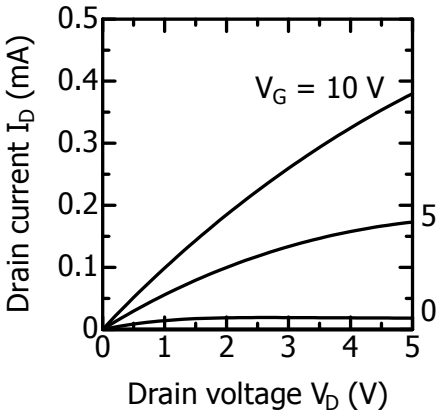

Fig. 2 Drain voltage vs drain current characteristics.

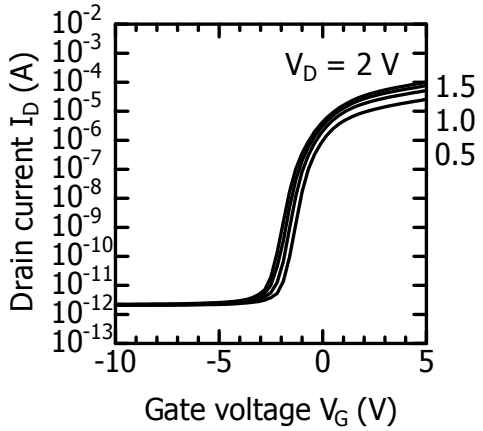

Fig. 3 Gate voltage vs drain current characteristics.

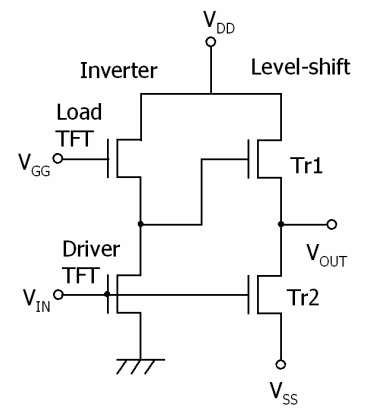

Fig. 4 Level-shift inverter with super-buffer configuration.

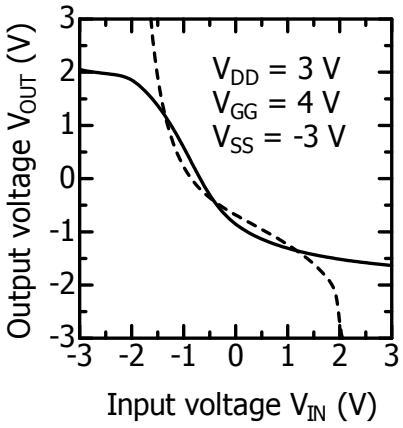

Fig. 5 Transfer curve of level-shift inverter.

3. Static Characteristic of Transistor

Figures 2 and 3 show drain voltage (V_D) vs drain current (I_D) and gate voltage (V_G) vs drain current (I_D) characteristics, respectively. The channel length was 50 µm and the channel width was 150 µm. N-channel depletion mode transistor was obtained and estimated field-effect mobility (μ_{FE}) was 21 cm^2/Vs from curve fitting in Fig. 2. The on/off ratio was 10^7, the threshold voltage was -2 V, and the subthreshold swing was 0.26 V/decade. In Fig. 3, a turn-on behavior of a subthreshold region was changed by changing the drain voltage. The reason is unknown, however, back-gate effects is one of the possible reason.

4. Integrated circuit with SA-IZOTFT

Figure 4 shows an inverter circuit with a level-shift under study. Driver transistor at inverter stage and a gate electrode of level-shift stage are connected in a same wire, i.e., super-buffer configuration is applied to this circuit.[9] In this configuration, shape of transfer curve becomes complex, however, larger gain could be realized by applying anti-phase signals to upper and lower level-shift IZO TFTs. Therefore, a larger logic swing can be obtained, and it is possible to correspond to a wide difference of the threshold voltage. By adjusting a ratio of level-shift circuit as unity, faster carrier injection and extraction could be realized, i.e., faster response is achieved. Channel length was 3 µm, and a ratio of this inverter was 10. Figure 5 shows input vs output voltage characteristics of the level-shift inverter, as shown in Fig. 4. Gain of 1.8 and logic swing of 2.5 V were obtained in this characteristics. Therefore, comparably wider logic swing can be obtained nevertheless the use of depletion-mode TFT.

5. Conclusions

We have fabricated the SA-IZO TFT using back-surface exposure. Excellent transistor characteristic was obtained, and the operation of the level shift inverter was well carried out. Our issues are control of the threshold voltage, an improvement of the mobility, and operation of the ring oscillator and amplification circuit.

References

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