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Realizing High Quality Metal-Gate/High-Permittivity Dielectric Stack on Indium Gallium Arsenide by Vacuum Annealing and Silane Treatment

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1. INTRODUCTION

High mobility III-V compound semiconductors have received renewed interest as alternative materials to replace conventional Si or strained Si channels and to be heterogeneously integrated on Si or silicon-on-insulator substrates for advanced CMOS technology beyond the 22 nm technology node. However, the lack of high quality and thermodynamically stable gate dielectrics on III-V similar to that of SiO_2 on Si remains a major challenge to the development of well-tempered III-V MOSFET technology. Exposure of III-V to air or low vacuum results in the rapid formation of a low quality native oxide on the surface, leading to Fermi level pinning and high interface state density [1-2]. We have recently demonstrated high quality gate stack formation on GaAs using *in-situ* surface passivation technology [3]. This surface passivation technology is compatible and can be integrated with a matured high-*k* gate dielectric process module. With higher electron mobility than GaAs, InGaAs is perhaps even more attractive for high speed CMOS applications. Nevertheless, the *in-situ* surface passivation technology has not been investigated on InGaAs.

In this paper, we report the first investigation of the effectiveness of *in-situ* surface passivation technology (vacuum annealing (VA) and silane (SiH_4) treatment) on InGaAs. By incorporating *in-situ* surface passivation technology during TaN/HfAlO/InGaAs stack formation, excellent *C-V* characteristics with low frequency dispersion, small stretch-out and interface state density D_{it} as low as $3.5 \times 10^{11} – 5.0 \times 10^{11}$ $cm^{-2}eV^{-1}$ can be achieved on InGaAs.

2. EXPERIMENT

The process sequence for device fabrication is depicted in Fig. 1 (a). P-type Zn-doped GaAs (100) wafers with doping concentration N_A of 1-5 $\times 10^{16}$ cm^{-3} were used as the starting material. 100 nm of Zn-doped GaAs buffer layer with N_A of 1×10^{17} cm^{-3} and 15 nm of Zn-doped $In_{0.18}Ga_{0.82}As$ layer with N_A of 1×10^{17} cm^{-3} were subsequently grown by metal-organic chemical vapor deposition (MOCVD). Pre-gate wet chemical cleaning process employed HCl and NH_4OH for native oxide and excess elemental As removal respectively, followed by $(NH_4)_2S$ for *ex-situ* surface passivation to prevent the growth of native oxide. After wet cleaning, the wafers were quickly loaded into a multi-chamber gate cluster system, where 600 ˚C baking under high vacuum for native oxide decomposition, SiH_4 treatment at 300 ˚C – 500 ˚C for surface passivation and MOCVD high-*k* dielectric (HfAlO) deposition were carried out, as illustrated by Fig. 1(b). The high vacuum transfer module serves to prevent wafers from exposure to low vacuum or atmosphere. On a control wafer, VA and SiH_4 treatment steps were skipped. Post deposition anneal (PDA) at 500 ˚C for 60 s was then performed to improve the quality of as-deposited HfAlO film. After reactive sputter deposition of TaN metal gate and gate patterning, the fabrication process was completed with forming gas anneal.

3. RESULTS AND DISCUSSION

X-ray rocking curve of the (004) reflection on the InGaAs/GaAs structure reveals the high crystalline quality of the InGaAs layer grown by MOCVD process (Fig. 2). The composition of indium is ~ 18 %. Due to lattice-mismatch, the InGaAs film is under compressive strain. Atomic force micrographs in Fig. 3 illustrate that the surface roughness of GaAs can be maintained during MOCVD III-V epitaxial process. Fig. 4 shows the schematic and cross-sectional transmission electron microscopy (TEM) micrograph of a completed TaN/HfAlO/$In_{0.18}Ga_{0.82}As$ stack with VA and SiH_4 treatment. An oxidized Si layer was formed between HfAlO and $In_{0.18}Ga_{0.82}As$, replacing poor quality native oxide. Diffractogram obtained at the $In_{0.18}Ga_{0.82}As$ layer reveals excellent crystalline quality [inset of Fig. 4 (b)].

Effect of wet chemical cleaning and air exposure duration on native oxide thickness was investigated by using ellipsometer, as summarized in Fig. 5. HCl is effective for native oxide removal on InGaAs. However, rapid growth of native oxide upon exposure to atmosphere was observed. The interval between different chemical cleaning steps should be minimized to suppress the native oxide growth. Significant reduction in the growth rate of native oxide was also observed after $(NH_4)_2S$ treatment. XPS spectra of As 3*d* in Fig. 6 show the elimination of As-O bond after VA and SiH_4 treatment during gate stack formation. The completely removal of arsenic oxide contributes to drastic improvement in *C-V* characteristics of InGaAs capacitors. Fig. 7 plots the *C-V* characteristics at measuring frequency of 10 kHz, 100 kHz, and 1 MHz. Negligible frequency dispersion was observed, as compared to the control capacitors without VA and SiH_4 treatment. *C-V* forward- and reverse-sweeps of InGaAs capacitors in Fig. 8 highlights the improvement in hysteresis after additional VA and SiH_4 treatment. Using SiH_4 treatment at higher temperature, hysteresis can also be further improved (inset of Fig. 8). Fig. 9 plots the gate leakage current density J_G obtained at $V_G = V_{fb} - 1$ V as a function of EOT. The samples without VA and SiH_4 treatment demonstrate higher J_G. This is probably attributed to the formation of traps within the bandgap due to the desorption of volatile Ga and/or As oxide and the out-diffusion of Ga and/or As into HfAlO gate dielectric. The *in-situ* surface passivated InGaAs capacitors exhibit similar gate leakage to GaAs capacitors. With EOT of 2.3 nm, the InGaAs MOS capacitor demonstrates a low J_G of 1.54×10^{-5} A/cm^2 at $V_G = V_{fb} - 1$ V. D_{it} was evaluated by using conductance method and summarized in Fig. 10. The D_{it} level in InGaAs capacitors is similar to that in GaAs capacitors, indicating that the presence of indium does not affect the overall gate stack integrity. Further improvement in D_{it} can be achieved by applying higher SiH_4 treatment temperature, and D_{it} as low as $3.5 \times 10^{11} – 5.0 \times 10^{11}$ $cm^{-2}eV^{-1}$ can be achieved by using an optimal SiH_4 treatment at 500 ˚C.

4. SUMMARY

In summary, *in-situ* surface passivation technology (VA and SiH_4 treatment) was integrated to form high quality MOS gate stack on InGaAs for the first time. With additional VA and SiH_4 treatment, the $In_{0.18}Ga_{0.82}As$ capacitors with EOT of 2.3 nm demonstrate superior *C-V* characteristics with D_{it} as low as $3.5 \times 10^{11} – 5.0 \times 10^{11}$ $cm^{-2}eV^{-1}$ and low J_G of 1.54×10^{-5} A/cm^2 at $V_G = V_{fb} - 1$ V. The presence of indium was found to have negligible negative impact on the gate stack integrity, indicating the potential applications of this effective surface passivation technology to InGaAs materials with even higher indium composition for higher mobility.

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References

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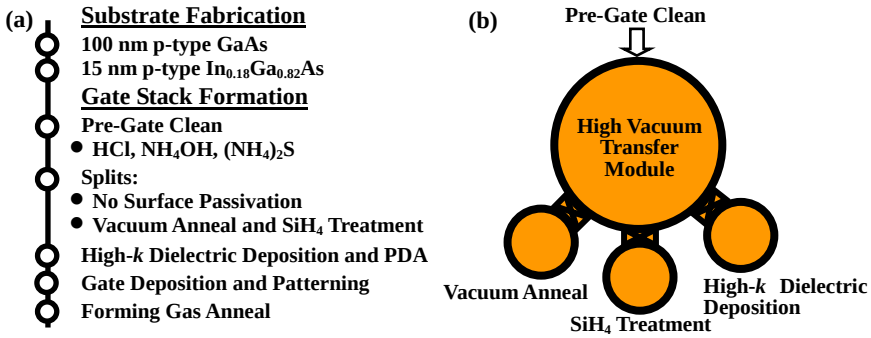

Fig. 1. (a) Process flow for fabrication of $In_{0.18}Ga_{0.82}As$/GaAs substrates and integration of VA and SiH_4 treatment during gate stack formation. (b) Schematic illustrating the multi-chamber gate cluster system used for surface passivation in this work. The high vacuum transfer module plays a significant role in reducing native oxide formation during wafer transfer.

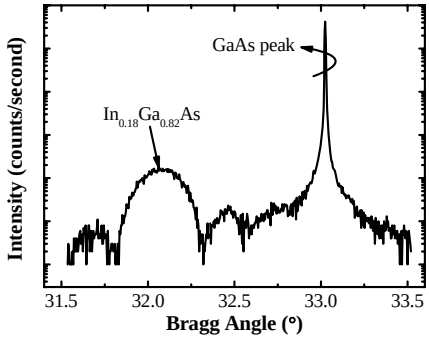

Fig. 2. X-ray rocking curve of the (004) reflection on the $In_{0.18}Ga_{0.82}As$/GaAs structure, showing high crystalline quality of the InGaAs layer.

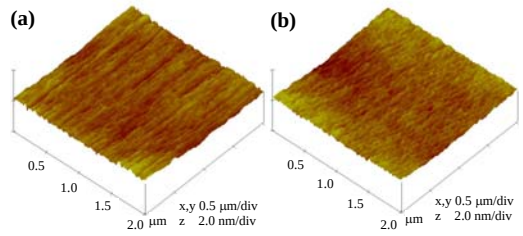

Fig. 3. AFM images of (a) GaAs before III-V growth (RMS = 1.1 Å), and (b) $In_{0.18}Ga_{0.82}As$/GaAs structure (RMS = 1.3 Å). The surface roughness can be maintained during the MOCVD III-V epitaxial process.

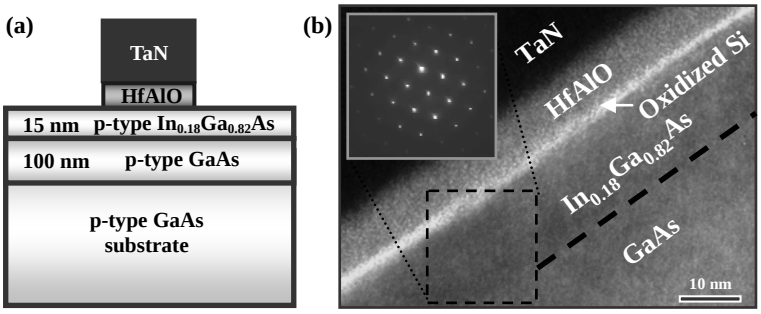

Fig. 4. (a) Schematic of the InGaAs MOS structure, and (b) TEM micrograph showing the cross-section of a completed TaN/HfAlO/$In_{0.18}Ga_{0.82}As$ stack with VA and SiH_4 treatment. An oxidized Si layer was formed between HfAlO and InGaAs. Diffractogram in the inset reveals excellent crystalline quality of the $In_{0.18}Ga_{0.82}As$ layer.

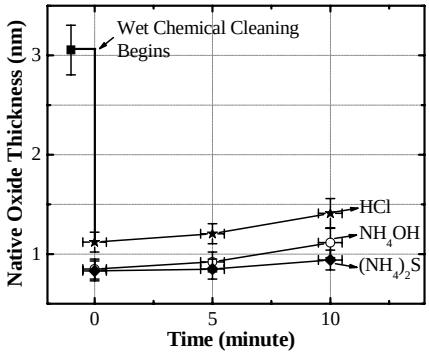

Fig. 5. Native oxide thickness as a function of air exposure duration. The air exposure interval between different cleaning steps should be minimized to reduce further growth of native oxide.

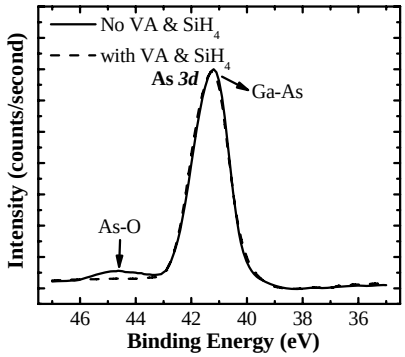

Fig. 6. Significant reduction in As-O signal was observed in the As *3d* XPS spectrum after VA and SiH_4 treatment.

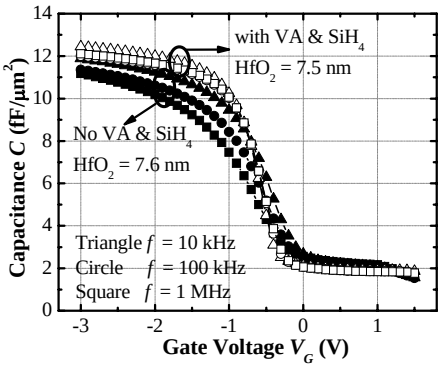

Fig. 7. *C-V* characteristics of InGaAs capacitors with and without VA and SiH_4 treatment at various frequencies. Additional VA and SiH_4 drastically suppress frequency dispersion.

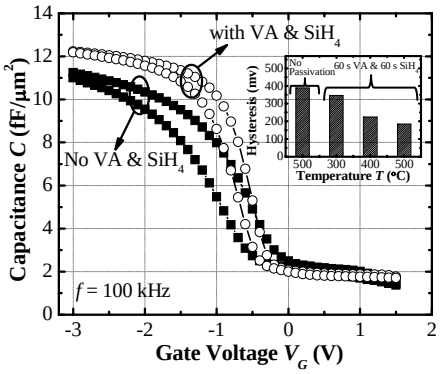

Fig. 8. Significant reduction in hysteresis can be achieved in *C-V* forward- and reverse-sweeps of InGaAs capacitors by integrating VA and SiH_4 treatment during gate stack formation.

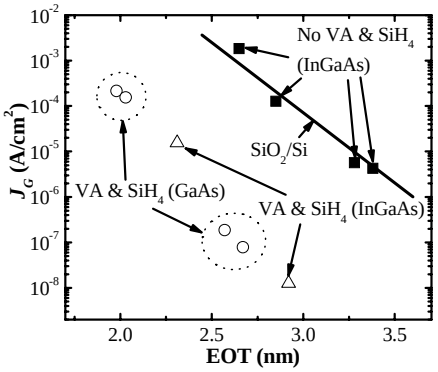

Fig. 9. The gate leakage current density J_G obtained at $V_G = V_{fb}$ - 1 V as a function of EOT.

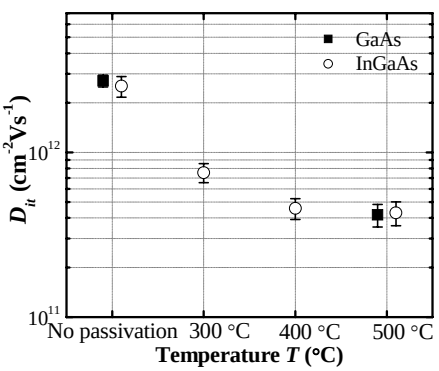

Fig. 10. Interface state densities D_{it} at various SiH_4 treatment temperatures. D_{it} as low as 3.5 × 10^{11} to 5.0 × 10^{11} $cm^{-2}eV^{-1}$ can be achieved with VA and SiH_4 treatment.