

Fabrication of III-V MOS structure by using selective oxidation of InAlAs

S. Nakagawa¹, M. Yokoyama¹, O. Ichikawa³, M. Hata³, M. Tanaka¹, M. Takenaka¹, S. Takagi^{1,2}

¹School of Engineering, ²Graduate School of Frontier Science, University of Tokyo, ³Sumitomo Chemical

7-3-1 Hongo, Bunkyo-ku, Tokyo 113-0032, Japan

Phone & Fax: +81-3- 5841-6733, E-mail: naka@mosfet.t.u-tokyo.ac.jp

1. Introduction

Recently a variety of new channel structures and materials have intensely been investigated because of the scaling limit of Si technology. For p-MOSFETs, many device concepts such as uni-axial compressive strain, (110) surfaces, and Ge channels have already been proposed and demonstrated. However, for n-MOSFETs there have currently been few promising device concepts since the tensile strain was introduced to Si channels. Although it is quite difficult to form high quality MOS interfaces of III-V semiconductors, the III-V MOSFETs have recently been expected to be a promising candidate of high performance n-MOSFETs because of these high electron mobilities.

In this paper, we present a selective oxidation technique of InAlAs [1] grown on an InP substrate for the III-V MOS structure. The selectively oxidized InAlAs formed the gate oxide and the InAlAs oxide/InP MOS structure exhibited an interface trap density of $10^{12} \sim 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$.

2. Experiments

The MOS structures were fabricated by using an InAlAs layer grown on an (100) n-InP substrate ($N_A = ? \text{ cm}^{-3}$) as shown in Fig. 1. The 10-nm lattice matched $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ layer was grown by molecular beam epitaxy (MBE) at the growth temperature of 500 °C. The wet thermal oxidation [2] was used to form the gate oxide because it can oxidize the InAlAs at low temperature. The InAlAs layer was selectively oxidized at 525°C in a furnace with a N_2 carrier gas bubbling H_2O at 85°C. After oxidation, Aluminum metal was deposited to form gate electrodes.

The oxidizing rate of the InAlAs was measured by an ellipsometer and a stylus surface profiler. The composition of the oxidized layer was evaluated by TEM and XPS analyses. The electrical characteristics of the fabricated MOS structure were evaluated by I-V and C-V measurements. The interface trap density and the time constant of the MOS interface state were evaluated by the conductance method. The capture cross sections were also calculated by the measured time constant.

3. Results and Discussion

For the measurement of the oxidizing rate, we prepared a 50nm InAlAs grown on InP substrate. The oxidized depth as a function of the oxidation time is shown in Fig. 2. This result shows that the InAlAs layer was selectively oxidized because the oxidized depth was saturated at 50 nm.

A cross section TEM image of the MOS structure is

shown in Fig. 3. It can be seen that the InAlAs was oxidized uniformly. The composition of oxidized films was evaluated by the XPS analyses as shown in Fig. 4. The Ar sputter was used during the XPS measurements to evaluate the composition at each depth. Figure 4 shows that the oxidized film consisted of In-Ox, Al-Ox and P-Ox and As near the InAlAs-Ox/InP interface. The P and As atoms moved during the oxidation. Especially the most As atoms in the InAlAs layer evaporated from the InAlAs-Ox.

The measured I-V characteristic of the InAlAs-Ox/InP MOS structure is shown in Fig. 5. The gate leak current was decreased as increasing the oxidation time. The C-V and G-V characteristic of the MOS capacitor with 60 min oxidation time were measured to evaluate the MOS interface. The C-V characteristics at 1MHz, 500kHz, 50kHz and 5kHz were shown in Fig. 6. Although all the capacitances were not saturated at the accumulation region, the inversion region (weak inversion) and the small frequency dispersion were observed, suggesting low interface trap density. The conductance peaks with the gate bias of -0.1V to 0.4V were shown in Fig. 7. The Interface trap density was evaluated by the conductance method with the surface potential fluctuation model [3] as shown in Fig. 8. The MOS interface trap density was extracted to be around $10^{12} \text{ eV}^{-1} \text{ cm}^{-2} \sim 10^{13} \text{ eV}^{-1} \text{ cm}^{-2}$. The time constant of interface state τ_n is evaluated from the conductance peak as shown in Fig. 9. It is found the slope of the time constant in the logarithm plot increased with the energy level. Generally, n-MOSFETs time constant is known to be described by

$$\tau_n = \frac{1}{\sigma V_{th} N_B} \exp \left[\frac{-q(E_f - E_c)}{kT} \right] \quad (1)$$

(σ : captured cross section, V_{th} : carrier thermal velocity, and N_B : contaminant concentration of bulk)

Therefore the capture cross section of the interface state can be calculated from the time constant as shown in Fig. 10. The calculated capture cross sections were around $10^{-12} \sim 10^{-14} \text{ cm}^2$. Electron traps with this capture cross section size is popularly known as Coulomb-attractive traps [4].

4. Conclusion

In this paper, the selective wet oxidation technique of InAlAs was presented to form the InAlAs-Ox/InP MOS structure. The fabricated MOS structure exhibited the low frequency dispersion C-V characteristic with the interface

trap density of around $10^{12}\text{eV}^{-1}\text{cm}^{-2} \sim 10^{13}\text{eV}^{-1}\text{cm}^{-2}$. The demonstrated approach will be a promising candidate to form a high quality III-V MOS interface.

Acknowledgment This work was partly supported by NEDO/MIRAI project and a Grant-in-Aid for Scientific Research on Priority Area (No. 19860024) from the Ministry of Education, Culture, Sports, Science, and Technology in Japan.

References [1] N. Iwai et al. IEEE (1998) [2] H. Takenouchi et al. Electronics Letters (29th August 1996) Vol.

32 No. 18 [3] J. R. Brews et al., Solid-State Elec.(1983) vol. 26 No.8 [4] T. Taur, T. H. Ning, Fundamentals of modern VLSI devices, Cambridge

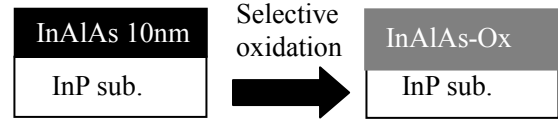


Fig.1 The MOS structure formed by selective oxidation of InAlAs.

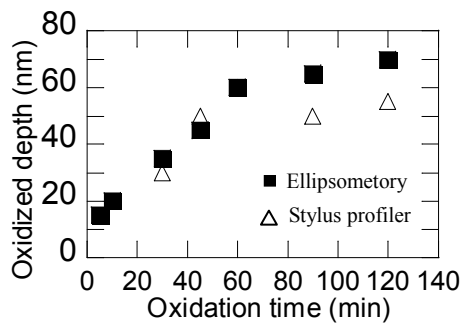


Fig.2 The oxidized depth vs. oxidation time determined by an ellipsometry and stylus profiler.

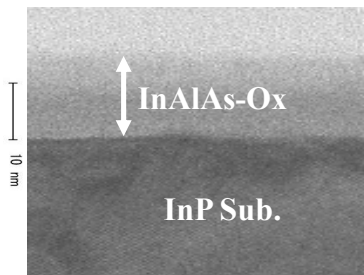


Fig.3 TEM image of InAlAs-Ox/InP MOS structure with 60 min oxidation time.

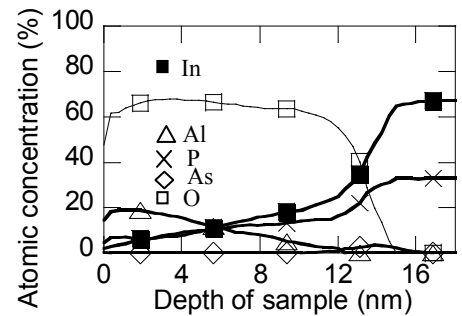


Fig.4 Atomic concentration vs. sample depth evaluated by XPS analyses

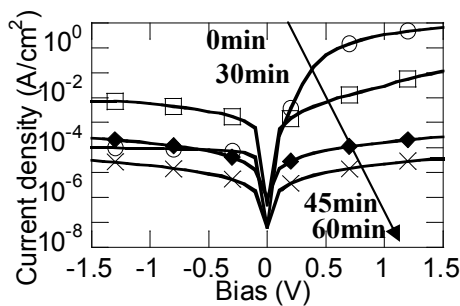


Fig.5 I-V characteristic with oxidation times of 0min, 30min, 45min, and 60min.

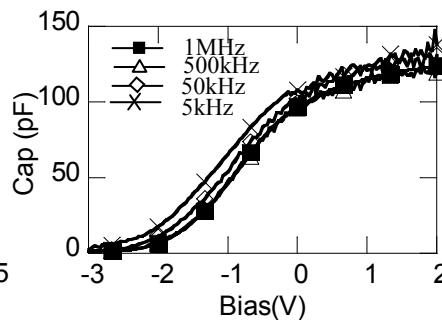


Fig.6 C-V characteristic of the InAlAs-Ox/InP MOS with the oxidation time of 60min.

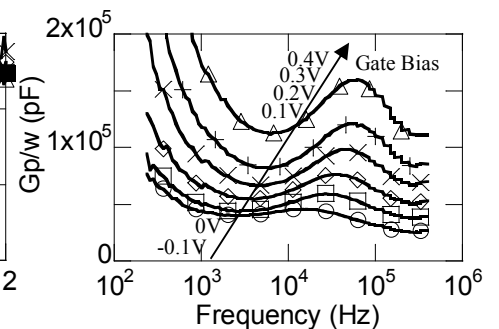


Fig.7 Gp/w vs. frequency of the InAlAs-Ox/InP MOS with the oxidation time of 60min.

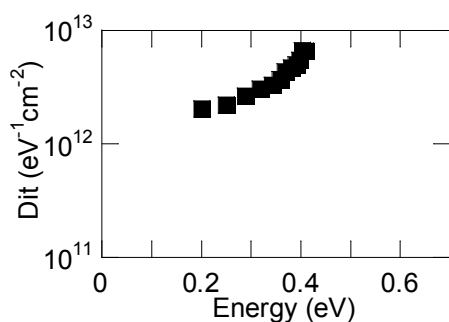


Fig.8 Energy distribution of interface state densities of sample determined by the conductance method

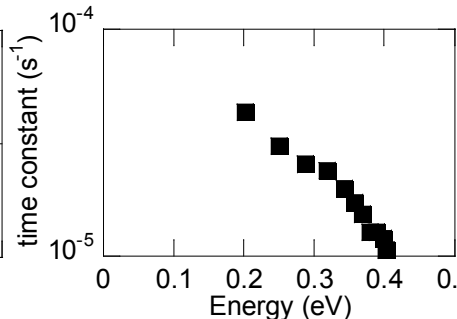


Fig.9 Energy distribution of the time constant of the interface states determined by peak frequencies of the conductance curves.

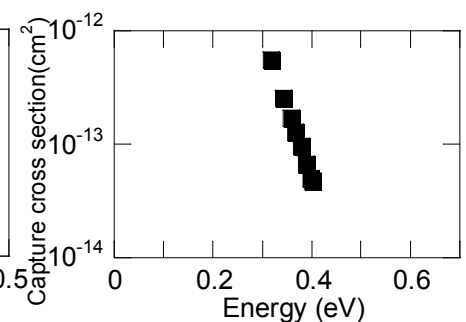


Fig.10 Energy distribution of the capture cross section determined by the time constants of the interface states.