Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 1064-1065

G-9-6

GaAs MOS Diodes with the Gate Oxide Formed by PEC Method

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1. Introduction

In past decade, many research teams have made great efforts to improve the performances of the GaAs metal-oxide-semiconductor (MOS) devices. One of key problems is to get better gate insulator of the device. Generally, the gate insulators of GaAs MOS (MIS) devices were externally deposited dielectrics, such as Al_2O_3, SiO_2, Ga_2O_3 and so on [1-3]. Unfortunately, the quality of the device is limited by the interface contaminants between external deposited oxide and GaAs, which inherently exist on the surface of the GaAs wafer before insulator layer deposition. In order to avoid the influence of the contaminants originally existed on the GaAs surface, it is better to form the insulator layer via a chemical reaction with the component in the surface layer of GaAs. In this work, we investigated the performance of the GaAs MOS diodes in which the gate oxide was directly grown on the semiconductor surface using photoelectrochemical (PEC) oxidation method to replace the external deposited dielectrics.

2. Experimental procedure

The dependence of the growth rate on the pH value was first investigated. The PEC oxidation system included a He-Ne laser with a wavelength of 632.8 nm used as the light source, a pH meter for monitoring the pH value of the solution and an amperometer, which is connected between two Pt electrodes, of which one is contacted with the metal mask on the sample and the other is just immersed in the solution.

The GaAs samples used in this work were grown by using a metal-organic chemical vapor deposition (MOCVD) system. A 400nm-thick undoped GaAs was grown as the buffer layer, followed by the growth of an 1μm-thick n-type GaAs (4×10^{17} cm^{-3}). The sample surface other than the central circular area was covered with a AuGeNi/Au metal mask (see inset of Fig.1) for electric contact with the Pt electrode. The diluted HCl was used as the electrolytic solution. During the PEC process the GaAs samples dipped in the solution were illuminated with a He-Ne laser of an intensity of 6.8 mW/cm^2 for 30min to induce the PEC reaction on the GaAs surface. Most of the samples were then thermally treated at 200, 300 and 400°C in O_2 ambiance for 10, 20, 30 and 40 min at each temperature.

To realize the composition and the structure of the resulted layers both the as-grown and heat treated samples were then characterized with various measurements such as the X-ray photoelectron spectroscopy (XPS) and glancing incident angle X-ray diffraction (GIXRD). The GaAs MOS diodes were then fabricated and characterized. to investigate surface state density between the interface of GaAs and GaAs PEC oxide.

3. Experimental results and discussion

The XPS spectra of the core-level Ga3d and As3d of the GaAs oxide films were analyzed. Fig. 1(a) shows the XPS spectra of Ga3d, from which it can be seen that for the as-grown sample the Ga3d spectrum is composed of two bands located at 21 eV and 19.4 eV, corresponding to Ga_2O_3 and GaAs, respectively. But for samples annealed in O_2 ambient at temperatures 200, 300 and 400°C only the Ga_2O_3 signal exists in the spectra. Similarly, as shown in Fig. 1(b), the spectrum of As3d of as-grown sample contains two bands at 44.9 eV and 41 eV, which correspond to As_2O_3 and GaAs, respectively, but only the As_2O_3 signal exists in the spectra of the heat treated oxide films. These results indicate that the layer formed at the surface of GaAs by PEC method is really an oxide film of Ga and As.

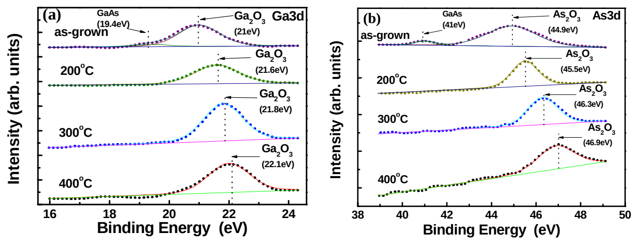

Fig.1 XPS spectra for the core-level (a) Ga3d and (b) As3d of the PEC oxide layers, as-grown and annealed at various temperatures for 30 min.

The glancing incident angle X-ray diffraction (GIXRD) measurement gives further information about the crystallography of the resulted GaAs oxide film. Figure 2 shows the diffraction patterns of the GaAs oxide films formed by PEC method. It can be seen that for the as-grown GaAs oxide film, no diffraction peaks can be found. It indicates that the as-grown oxide film has an amorphous structure. But the peaks of (401) Ga_2O_3, (111) β-Ga_2O_3 and (210) As_2O_3 occurred in the GIXRD spectra of the samples annealed at temperature 300°C and 400°C. It indicates that the microstructure of the oxide films changed from an amorphous to a polycrystalline phase by the thermal treatment.

The resulted GaAs oxide films were then used as the gate oxides layers of GaAs MOS diodes, as shown in Fig. 3. For device fabrication, a 10 nm thick SiO_2 layers were deposited on the GaAs oxide layers to protect the oxide layers because the GaAs oxide films easily dissolve in the developer solution. Four MOS diodes were fabricated, named as

No. 1~4. Table I shows the parameters of the gate oxides of these diodes. In all the cases the thickness of the as-grown oxide film was the same and decreased with increasing the annealing temperature, indicating that the oxide layer became denser.

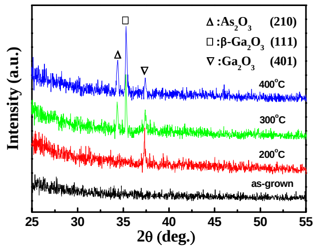

Fig. 2 X-ray diffraction patterns of the PEC oxide layers, as-grown and annealed at various temperatures for 30 min.

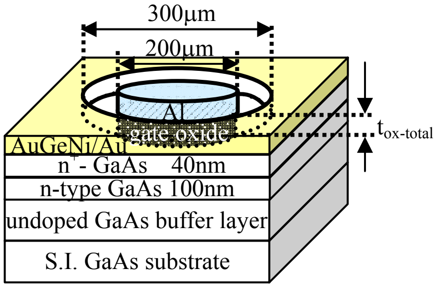

Fig. 3 The schematic cross-sectional of MOS diodes.

Table I The parameters of the gate oxides of the diodes.

No.	Oxide structure	t_{SiO2} (nm)	$t_{ox\text{-}PEC}$(nm) (non-annealing)	GaAs oxide (annealing Temp.)(°C)	$t_{ox\text{-}PEC}$ (nm) (after annealing)	$t_{ox\text{-}total}$ (nm)
1	SiO_2+ GaAs oxide	10	40	No annealing	40	50
2	SiO_2+ GaAs oxide	10	40	200	33.6	43.6
3	SiO_2+ GaAs oxide	10	40	300	26.4	36.4
4	SiO_2+ GaAs oxide	10	40	400	22.8	32.8

Figure 4 shows the current-voltage characteristics of the GaAs MOS diodes. For all the four diodes, the forward gate leakage current is lager than reverse gate leakage current, and the forward breakdown voltage is smaller than the reverse breakdown voltage. This is due to the fact that a lot of electrons accumulated at the interface between the GaAs oxide and n-GaAs, which leads to the increase of the forward leakage current. The breakdown voltage is defined as the voltage at which the sloped straight line of the corresponding leakage current intersects the voltage axis. The reverse breakdown voltages of diodes No. 1~4 are -19.1, -23.2, -28.1, and -29.4V, and the corresponding breakdown fields are 3.82, 5.30, 7.72, and 8.96MV/cm, respectively. From the measurement results, the No. 4 GaAs MOS diode has better performance. It can be explained that the GaAs oxide film changed from an amorphous to a polycrystalline phase and became denser by the thermal treatment.

To investigate the interface state density, the capacitance-voltage (C-V) characteristics of the MOS diodes were measured. Figure 5 shows the result for diode No. 4. The interface state density D_{it} can be estimated from $D_{it}=(C_{ox}\Delta V_{th}/AqE_g)$, where the C_{ox}=77.1pF are capacitances of the gate oxide of the diode, A=3.14×$10^{-4}$$cm^2$ is oxide area, q is the electron charge, E_g=1.42eV is the energy gap of n-type GaAs, and ΔV_{th}=0.69V is the voltage shift of the diode due to the different charging conditions of deep-lying interface states. For the C-V characteristic shown in Fig. 5, the interface state density of the diode No. 4 is 7.45×10^{11}/cm^2eV. Similarly, the interface state density for the diodes No. 1, 2 and 3 are 7.85×10^{11}/cm^2eV, 7.47×10^{11}/cm^2eV and 7.28×10^{11}/cm^2eV, respectively.

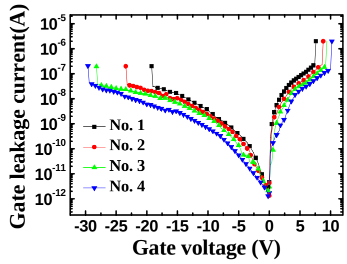

Fig. 4 The current-voltage characteristics of diodes No. 1~4.

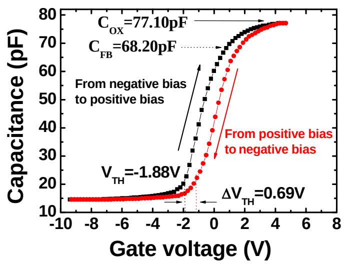

Fig. 5 The capacitance-voltage characteristics of the MOS diode No. 4.

4. Conclusion

We successfully used PEC oxidation method to directly grow oxide layer on GaAs surface, forming a high quality oxide as the gate oxide for the GaAs MOS diodes. The GaAs oxide films without and with thermal treatment at 200, 300, and 400°C were characterized by X-ray photoelectron spectroscopy and glancing incident angle X-ray diffraction. The interface state density of the MOS diodes No. 1~4 are 7.85×10^{11}/cm^2eV, 7.47×10^{11}/cm^2eV, 7.28×10^{11}/cm^2eV, and 7.45×10^{11}/cm^2eV, respectively. The result of the paper indicates that the method used in the work is promising for application in the III-V-based integrated circuit using MOSFETs.

Acknowledgements

This work was supported by the National Sciences Council of the Republic of China under contract number NSC 95-2221-E-150-083.

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