H-1-1 (Invited)

# Nanowire Impact Ionization Transistors (I-FETs)

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**Abstract**

The Impact Ionization Nanowire Multiple-gate Field-Effect Transistor (I-FinFET or I-FET) is investigated. The multiple-gate structure enhances the impact ionization rate in the fin/nanowire, reduces the breakdown voltage $V_{BD}$ and improves device performance. A SiGe Impact Ionization Region (I-Region) is integrated on a Si or $Si_{0.75}Ge_{0.25}$ nanowire to enhance performance and $V_{BD}$. Complementary pair of I-FinFETs were realized. Excellent subthreshold swing of sub-5 mV/decade at room temperature was achieved. The lower electron and hole impact-ionization threshold energy of SiGe greatly enhances the drive current of n- and p-channel devices. A low $V_{BD}$ of -4.75 V is achieved for SiGe nanowire device. Challenges faced by I-MOS will be discussed.

## 1. Introduction

With supply voltage $V_{DD}$ reduction in conventional CMOS limited by the non-scalability of the subthreshold swing $S$, there is growing interest in an alternative electronic device with a steep subthreshold $S$. The impact ionization MOS field-effect (I-MOS) transistor has attracted interest (Fig. 1) [1]-[8]. It is a gated p-i-n diode with an impact ionization region (I-region) for gate-controlled avalanche of carriers. Devices with sub-20 mV/decade have been demonstrated using various fabrication schemes. A L-shaped I-MOS (LI-MOS) with good compactness, scalable I-region, and CMOS process-compatibility, was demonstrated with sub-5 mV/decade swing [3].

In this paper, we review our latest findings on I-MOS transistor or I-FET. N- and p-channel nanowire Impact Ionization multiple-gate transistor (I-MuGFET, I-FinFET, or simply I-FET) with subthreshold swing of less than 3 mV/decade at room temperature will be discussed. The multiple-gate architecture enhances gate control on the potential throughout the I-region, increases the lateral electric field and therefore the impact-ionization rate. Hence, the breakdown voltage $V_{BD}$ could be reduced, leading to a lower source bias needed to sustain impact-ionization. The increased gate-to-channel coupling effect enhances carrier multiplication, and improves the drive current for n- and p-channel devices.

## 2. Device Fabrication and Integration

The I-FET is CMOS process-compatible, and can be fabricated using a process flow shown in Fig. 2. 8-inch SOI or SGOI wafers were employed as starting substrates. Si or $Si_{0.75}Ge_{0.25}$ active regions were patterned using 248 nm lithography. Poly-Si/ $SiO_2$ gate stack with a $SiO_2$ hardmask was formed. Drain extension implant was performed to form a lightly-doped drain. This was followed by SiN spacer formation. The spacer size determines the dimension of the I-region. Selective epitaxial growth (SEG) formed part of the I-region as well. Integration of SiGe or Si in the source was done. The asymmetrical drain and source were implanted using separate masks with the opposite side covered by photoresist. Dopant activation, contact, and metallization were done. N- and p- channel nanowire I-MOS devices with gate length $L_G$ down to 50 nm were fabricated. The I-region length $L_I$ is ~ 40 nm.

## 3. Device Characteristics, Enhancement, and Challenges

### *A. Bandgap/Materials Engineering for Device Enhancement*

The breakdown characteristics for n-channel I-FETs are shown in Fig. 3. Steeper $I_D$-$V_S$ slope and lower $V_{BD}$ are observed for I-FETs with SiGe I-region as compared with devices with Si I-region. This is due to lower impact-ionization threshold energy for both electrons and holes, which induce early breakdown and larger electron-hole pair multiplication rate. Strain and bandgap engineering in such a structure reduces $V_{BD}$ and enhances device performance. With the same $V_S$ and $V_D$, the $I_{on}$ and maximum transconductance $G_m$ are enhanced by 2-3 fold in SiGe I-FETs due to the increased impact-ionization rate (Fig. 4) over Si I-FETs. Subthreshold swing of sub-5 mV/decade are achieved. N-channel Si and SiGe I-FinFETs have a threshold voltage $V_T$ of 1.28 V and 0.46 V, respectively [Fig. 2(a)]. For a given $|V_S|$, higher $I_{off}$ in SiGe I-FETs is due to higher band-to-band tunneling resulting from the smaller $E_G$. For a fairer comparison, $V_T$ or $I_{off}$ should be matched and a higher $|V_S|$ is thus used for Si I-FinFETs to achieve the same $|V_T|$ as SiGe I-FETs. Higher $|V_S|$ increases the electric field in the I-region resulting in lower $|V_T|$ and higher $I_{off}$. At matched $V_T$, $I_{off}$ of Si I-FinFETs will be higher than SiGe I-FinFETs by 2 to 5 times [Fig. 5(a) and Fig. 6(a)]. The $I_{off}$-$I_{on}$ plots measured at various $|V_S|$ for the n- and p-channel devices with $L_G$ of 50 nm are depicted in Fig. 5(b) and Fig. 6(b), respectively. At matched $V_T$ or the same $I_{off}$, the $I_{on}$ of SiGe I-FinFETs is significantly enhanced. We have also recently realized strained p-channel I-FinFETs with *in situ* doped Si:C source formed on Si nanowire (Fig. 7).

### *B. Major Challenges*

Nevertheless, the I-MOS device faces several major challenges. A major problem is device reliability. Impact ionization generates hot carriers in the vicinity of the gate dielectric, leading to rapid device degradation. Fig. 8 shows that even repeated sweeps to obtain the $I_D$-$V_G$ plot could lead to large increase in the subthreshold swing. Another problem is the requirement of a fairly large source bias $|V_S|$ to sustain impact-ionization. While we have substantially reduced $|V_S|$ through adoption of strain and SiGe, it is still high. Recently, we identified a trade-off between $I_{off}$ and switching delay of I-MOS devices [8]. It takes substantial time in the order of ps (longer than a conventional MOSFET) for the I-MOS to switch-on (Fig. 9). Random distribution of the switching time due to stochastic carrier multiplication is also a fundamental problem.

## 3. Summary

Complementary impact-ionization nanowire multiple-gates FinFET (I-FinFET or I-FET) has been extensively investigated. The multiple-gate structure enhances the impact-ionization rate in the I-region. Strain engineering is effective in reducing the impact-ionization threshold energy and improving device performance. However, the I-MOS still suffers from fundamental problems such as device reliability, need for large source bias, and issues (e.g. substantial switching time) related to the stochastic carrier multiplication process.

**Acknowledgement.** Research grant from Agency for Science, Technology, and Research (A*STAR), and research facilities at A*STAR Institute of Microelectronics are acknowledged.

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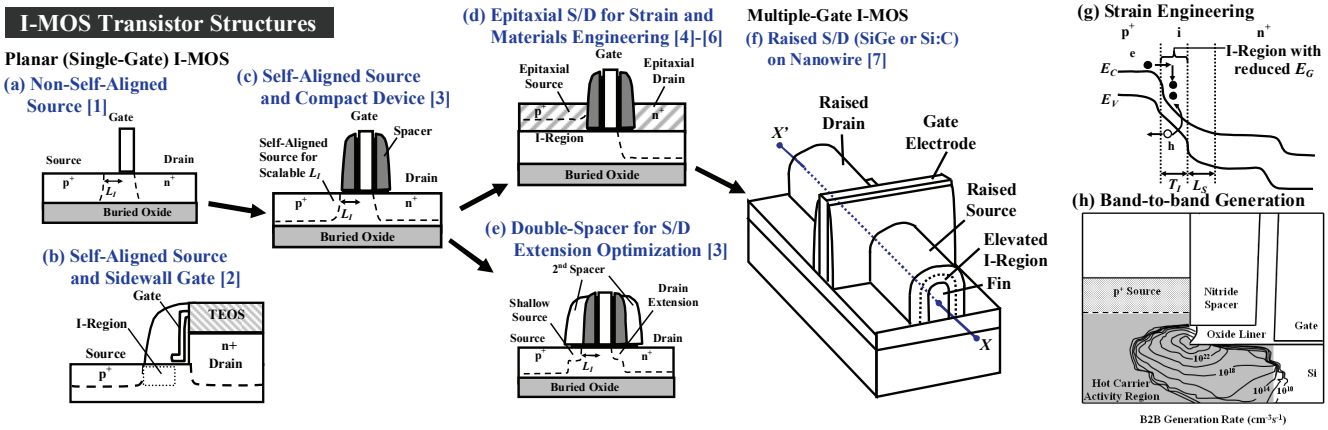


Fig. 1. Schematic of (a) non-self-aligned planar I-MOS [1], (b) I-MOS with a sidewall gate [2], (c) a planar IMOS with self-aligned source [3], (d) an IMOS with L-shaped I-region comprising epitaxial S/D for strain and materials engineering, and (e) a double-spacer IMOS which enables further device optimization [3], (f) a multiple-gate nanowire I-MOS [7]. Fig. 1(f) depicts the energy band diagram of an IMOS device in the on-state. (g) Strain engineering can reduce the bandgap $E_G$ in the I-region, and thus contributing to higher generation rate near the source, as illustrated in (h).

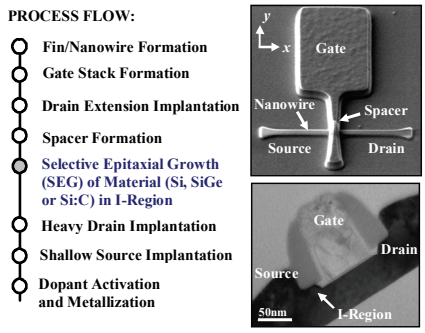


Fig. 2. Process flow for fabricating the nanowire I-MOS device, including selective Si or SiGe epitaxy to form part of the I-region. SEM and TEM images of device are also shown.

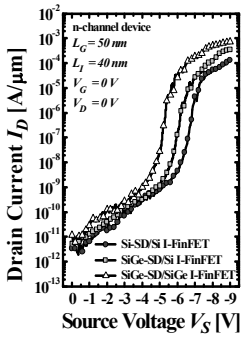


Fig. 3. $I_D$-$V_S$ plot for Si-SD/Si- nanowire I-FinFET, SiGe-SD/Si-nanowire I-FinFET and SiGe-SD/SiGe-nanowire I-FinFET.

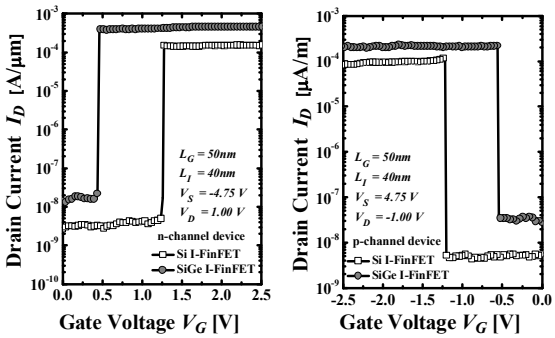


Fig. 4. $I_D$-$V_G$ plots of (a) n- and (b) p- channel devices with $L_G$ of 50 nm, I-region length $L_I$ of 40 nm, and EOT of ~3 nm. Si I-FET has Si raised S/D on Si nanowire, while SiGe I-FET has SiGe raised S/D on SiGe nanowire.

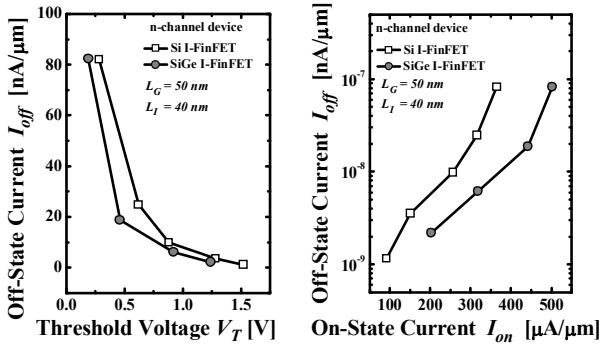


Fig. 5. (a) $I_{off}$ measured at ($V_G$–$V_T$) = -0.2 V as a function of $V_T$ for n-channel I-FinFET. (b) Measured $I_{off}$ - $I_{on}$ plot for the n-channel devices with varying $|V_S|$. $I_{on}$ is measured at ($V_G$–$V_T$) = 1.0 V.

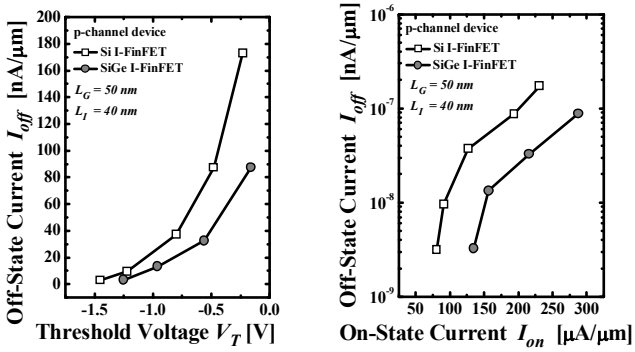


Fig. 6. (a) $I_{off}$ measured at ($V_G$–$V_T$) = +0.2 V as a function of $V_T$ for p-channel I-FinFET. (b) Plot of $I_{off}$ versus $I_{on}$ for the p-channel devices with various $|V_S|$. $I_{on}$ is measured at ($V_G$–$V_T$) = -1.0 V.

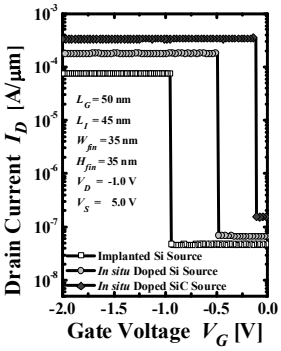


Fig. 7. $I_D$-$V_G$ plot of p-channel I-FETs with *in situ* doped Si:C S/D.

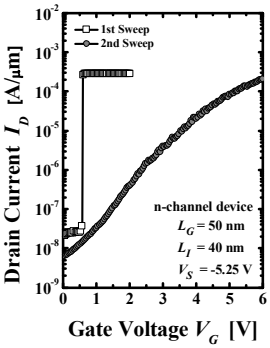


Fig. 8. $I_D$-$V_G$ cycling of I-MOS device usually leads to rapid device degradation.

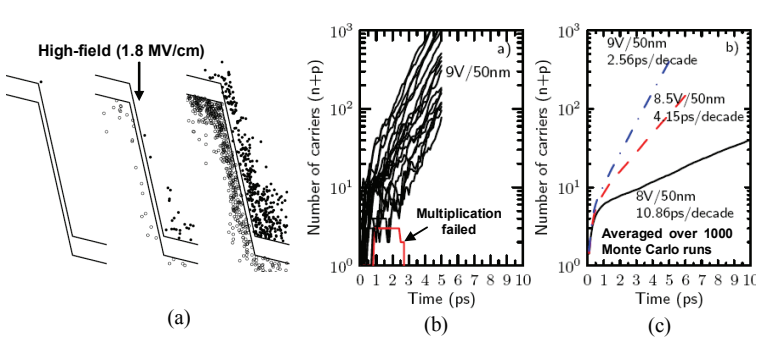


Fig. 9. (a) Injected of an electron into a high-field p-i-n region leads to a stochastic carrier multiplication process, where (b) the carrier number grows with time (20 Monte Carlo runs shown). (c) The growth rate increases with electric field.