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Fabrication of N-type and P-type Schottky barrier Thin-Film-Transistors crystallized by Excimer laser annealing and solid phase crystallization method

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1. Introduction

In Schottky barrier metal-oxide-semiconductor field effect transistors (SB-MOSFETs), source and drain (S/D) regions are formed with metallic junctions instead of impurity doped silicon. Therefore, SB-MOSFETs have numerous advantages including low temperature processing for S/D formation (less than 500 °C), simple fabrication process, low parasitic S/D resistance, short channel effect immunity and inherent physical scalability to sub-100 nm gate length [1]. Also SB-MOSFETs can easily employ high-k gate insulators and metal gate due to low temperature processing for S/D formation [2]. Based on these advantages, the SB-technology can apply to polycrystalline silicon thin-film-transistor (poly-Si TFT). Although poly-Si TFTs have lower device performances than the silicon-on-insulator (SOI) MOSFET, poly-Si TFTs have the advantage of stacked device structure, large area process, low cost and application of display [3]. In this paper, we fabricate the Er-silicided n-type and Pt-silicided p-type SB-TFTs on poly-Si film for application of system on glass (SOG) technology. High quality poly-Si Film was obtained by using excimer laser annealing (ELA) method or solid phase crystallization (SPC) method. Finally, the effect of forming gas anneal (FGA) was studied to improve the performance of SB-TFTs.

2. Experimental

Poly-Si SB-TFTs were fabricated with poly-Si film on insulator. The thermal oxide with 200 nm-thick was grown on (100) p-type bulk silicon wafer with 10~20 Ω -cm. And then the amorphous Si film with 100 nm-thick was deposited on thermal oxide by using low pressure chemical vapor deposition (LPCVD) at 530 °C. Amorphous Si was crystallized by using ELA method or SPC method. The energy density and process temperature of ELA is 400 mJ/cm² and 20 °C, respectively. SPC was carried out at 600 °C for 24 hour. After patterning active regions, a 5 nm-thick SiO₂ film was grown using thermal oxidation at 900 °C followed by depositing 100 nm-thick poly-Si for gate electrode. The photolithography combined with dry etching was employed to define a gate region. A sidewall spacer was formed using the thermal oxidation at a temperature of 900 °C and subsequent blanket dry etch processes. To fabricate the Er-silicided n-type and Pt-silicided p-type SB-TFTs, 50 nm-thick Er and Pt was deposited by RF magnetron sputter in Ar ambient. For formation of metal-silicided S/D junction, a thermally treatment process was carried out. The unreactive metal was removed. Finally, the fabricated poly-Si SB-TFTs were annealed in forming gas (2% H₂ in N₂) ambient at 450 °C for 30 min for improving the electrical characteristics.

3. Results and discussions

Fig. 1 shows the scanning electron microscope (SEM) image of poly-Si film. Poly-Si film obtained by ELA method has larger grain size than SPC method because the energy density of laser annealing is enough to melt the amorphous Si films. Furthermore, ELA method grows crystalline nucleus less than SPC method. Crystalline nucleus relate to crystallization temperature and grain size.

Fig. 2 represents the X-ray diffraction (XRD) results of poly-Si film. The poly-Si film expose peaks to (111), (220), and (311) crystal face. The intensity of XRD obtained from the ELA method is much stronger than SPC method. Therefore, it is concluded that poly-Si obtained by ELA method is superior to the SPC method.

The current-voltage (I-V) characteristics of SB-TFTs before and after FGA are shown in Fig. 3. I-V characteristics of SB-TFTs are classified with crystallization method of ELA and SPC. After FGA, the performances of SB-TFTs, such as I_D -V_G, I_D -V_D, and subthreshold swing (SS), considerably were improved by reduction of trap state at the poly-Si grain boundaries as well as interface trap state at gate oxide/poly-Si channel. As a result, SB-TFTs show high on/off current ratio larger than 10⁵ with low leakage current.

Table.1 summarizes the parameter value of SB-TFT with threshold voltage (V_{th}) and subthreshold swing (SS) before and after FGA.

4. Conclusions

In this work, we have fabricated the SB-TFTs on poly-Si film. High quality poly-Si films were obtained by

ELA and SPC methods. Fabricated SB-TFTs showed a low leakage current and a high on/off current ratio. After FGA, electrical characteristics were significantly improved due to reduction trap. Therefore, we can confirm application to display/memory integrated devices for SOG with SB-TFTs

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References

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Fig. 1 SEM image of poly-Si film with (a) ELA and (b) SPC.







2.0x10⁵ 1.8x10⁵ 1.8x10⁵ 1.4x10⁵ 1.4x10⁵ 1.4x10⁵ 1.2x10⁵ 1.0x10⁵ 2.0x10⁶ 0.0 -3 -2 -1 0 1 2 3

Drain voltage (V) (b) I_D-V_D curves of SB-TFTs by using ELA



(c) I_D -V_G curves of SB-TFTs by using SPC



(d) I_D - V_D curves of SB-TFTs by using SPC

Fig. 3 Current-voltage characteristics of fabricated SB-TFTs on poly-Si film obtained by ELA [(a) and (b)] and SPC [(c) and (d)].

ELA	SB-NTFT		SB-PTFT	
	Initial	FGA	Initial	FGA
$V_{th}(V)$	1.1	0.61	- 3.24	- 2.3
SS (mV/dec)	207	144	590	304
SPC	SB-NTFT		SB-PTFT	
	Initial	FGA	Initial	FGA
$V_{th}(V)$	2.27	1	- 2.96	-2.63
SS (mV/dec)	357	180	659	416

Table. 1 Electrical characteristics of SB-TFTs classified by crystallization method.