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# Novel F-shaped Triple Gate Structure for Improvement of Hot Carrier Reliability in Low Temperature poly-Si TFT

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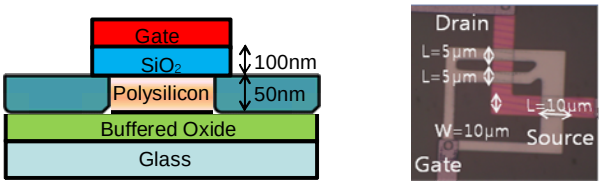
## 1. Introduction

Recently, low temperature polycrystalline silicon (poly-Si) thin film transistors (TFTs) have attracted a considerable attention for AMOLED (Active Matrix Organic Light Emitting Diode) in the pixel switching and peripheral circuit [1]. To employing poly-Si TFT to analog driving circuits and differential amplifier for high resolution display, high field mobility and stable saturation characteristics without kink current are required [2]. And the reliability of poly-Si TFT is also critical issue because the device in driving circuits should maintain its output current with accuracy during whole operation times. Hot carrier stress is usually used and investigated for verification of reliability.

The purpose of our work is to propose and fabricate a new F-shaped triple-gate structure for improvement of hot carrier reliability and suppression of kink current in low temperature poly-Si TFTs. Recently, sequential lateral solidification (SLS) crystallization has been developed to improve the mobility of poly-Si TFTs. It was reported in our previous paper that dual-gate and L-shaped dual gate could reduce the kink current of poly-Si TFTs [3]. However in that case, the difference in channel length between sub-TFTs should be large and kink current of TFTs still remains in part. The different channel structure is used in the proposed device to eliminate kink current effectively.

## 2. Device Fabrication

We have fabricated CMOS coplanar poly-Si TFT samples following the conventional top gate process as shown in Fig .1(a). First, a $SiO_2$ buffer layer is deposited on the glass substrate. And we deposited a 50-nm-thick amorphous silicon (a-Si) active layer by plasma enhanced chemical vapor deposition (PECVD). Then, the a-Si active layer was crystallized by the SLS method with a 308 nm XeCl excimer laser, and the silicon grain grew up in a fixed lateral direction.




(a) (b)

Fig. 1 (a) Cross Section View and (b) Plane View of F-shaped triple gate TFT fabricated by SLS Processed poly-Si TFT on glass substrate.

After the irradiation, a typical LTPS process sequences were followed. The F-shaped active patterning and gate patterning were adjusted to the lateral grain growth direction, as shown in Fig.1(b), and the fabricated TFTs contained two kinds of sub-TFTs; one had the channel in the perpendicular direction to the grain growth direction and the other had the channel in the parallel direction to the grain growth direction respectively. The (W/L) ratio of the poly-Si TFT is (10/20) μm.

## 3. Results and Discussions

Kink current due to an inherent floating body structure of thin film transistors plays a role in critical limit of actual operation [2]. Kink current is induced by impact ionization at the drain junction of the channel, due to a large drain field. So we have to design a novel structure with reducing an electric field near drain junction to suppress the kink current of TFT. Because the electric field is closely related with voltage drop, we have used a multiple-gate concept in order to make a smaller voltage drop at $TFT_2$ than other conventional gates as shown in Fig. 2.

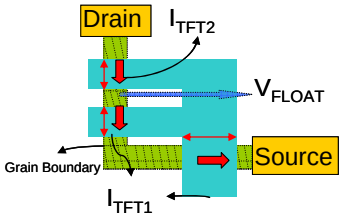



Fig. 2 Diagram of proposed F-shaped Triple Gate poly-Si TFT

To determine a total current of F-shaped TFT under high $V_{DS}$ condition, we assumed a relation with $TFT_1$ and $TFT_2$ as follows.

$$I_{TFT1}(\text{Linear}) = I_{TFT2}(\text{Saturation}) \quad \text{- (1)}$$

And then, we have analyzed the voltage of floating point to find a voltage drop across the $TFT_2$.

$$V_{float} = (1 - \frac{1}{\sqrt{1+(\frac{k_{TFT2}}{k_{TFT1}})}}) \cdot (V_G - V_T), \text{ where } k = \frac{W \cdot \mu \cdot C_{OX}}{2L} \quad \text{- (2)}$$

In equation (2), coefficient α is defined as a value of $k_{TFT2}$ divided by $k_{TFT1}$. So we have to increase the value of α as possible to get a larger value of $V_{float}$ reducing the electric field near drain junction. And then, we could set the other gates except $TFT_2$ into an equivalent model, that is, $TFT_1$ as shown in equation (3).

$$\frac{1}{k_{TFT_1}} = \frac{1}{k_{TFT_A}} + \frac{1}{k_{TFT_B}} + \frac{1}{k_{TFT_C}} + \cdots \quad \text{- (3)}$$

Based on this hypothesis, the value of α of proposed F-shaped triple gate is about 6.285, which is larger than that of dual-gate, L-shaped dual gate (about 1, 2.642 orderly). Therefore the proposed device successfully lowers electric field induced near drain junction. These results agree with a simulation results shown in

Fig 3. (Smart Spice 3.3 Versions.) And especially, comparing the applied drain voltages between drain region and sub-gate adjacent to drain region, we can find that F-shaped triple gate TFT could effectively lowers the induced drain bias than conventional gates, including a L-shaped dual gate in Fig. 3.

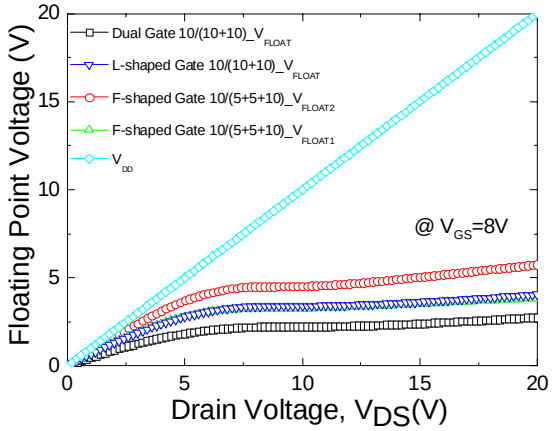



Fig. 3 Simulation Results : Floating Point Voltage ($V_{FLOAT}$) of a F-shaped Gate compared with other conventional Gate structures.

Fig. 4 shows the output characteristics of the proposed F-shaped triple gate and conventional single, dual-gate, L-shaped dual gate TFTs.

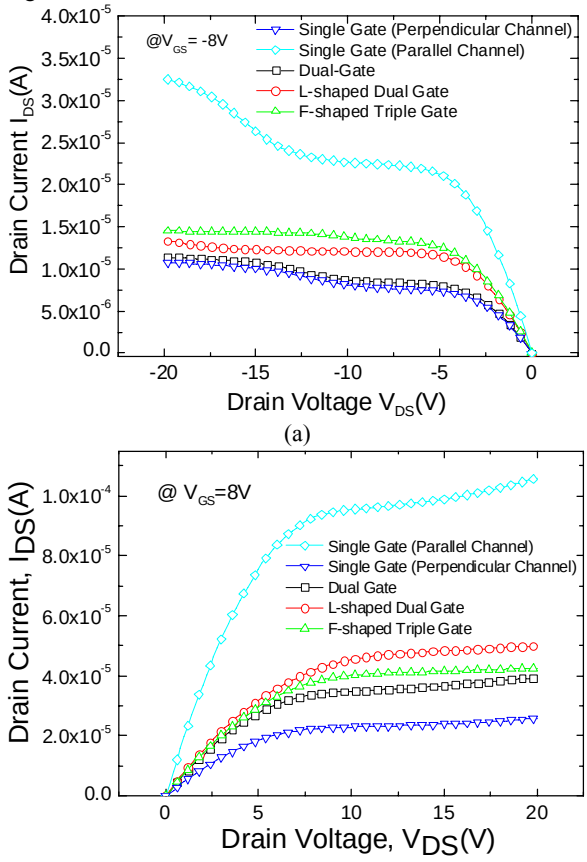



Fig. 4 Experimental Results : Output Characteristics of a (a) p-type (b) n-type F-shaped Gate poly-Si TFT compared with that of other conventional gate TFTs.

Due to the difference of floating voltage between F-shaped triple gate and other gate structures, the proposed device could exhibit a better saturation characteristic than the conventional single, dual-gate, L-shaped gate TFTs at a similar current. F-shaped triple gate shows a just 46% (n-type), 3% (p-type) of output conductance characteristic when comparing with L-shaped gate at $|V_{DS}|$=20V, $|V_{GS}|$=8V.

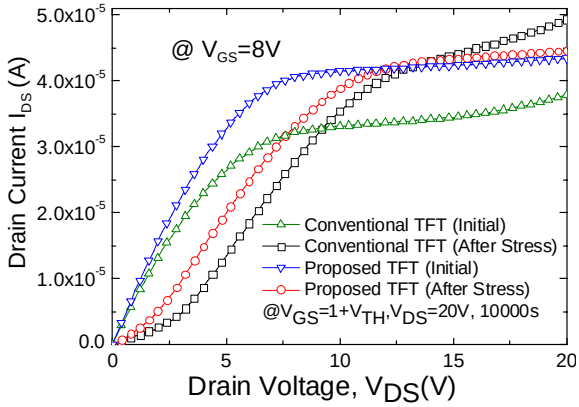



Fig 5. Output characteristics of TFTs before and after hot carrier stress ($V_{GS}=V_{TH}+1V$, $V_{DS}$=20V for 10,000s)

To investigate the reliability of F-shaped triple gate TFT, we have measured output characteristic of poly-Si TFTs with hot carrier stress according to stress times as shown in Fig. 5. Stress condition was $V_{GS} = V_{TH} + 1V$ and $V_{DS}$ = 20V for 10,000s. After the hot carrier stress, the output current of conventional TFT in the saturation regime was dramatically increased whereas that of proposed TFT in the saturation regime was rarely altered. This result was occurred due to the grain structure of poly-Si TFT.

There is a high correlation between the grain boundary structure near the drain junction and degradation of poly-Si TFTs [4]. Because the sub-TFT near drain junction in F-shaped triple gate TFT has almost parallel channel, it is more reliable under high drain field than the conventional gate TFT with sub-gate near drain junction which has perpendicular channel. For that reason, the stable saturation characteristic of the proposed F-shaped triple gate TFT has been maintained during hot carrier stress compared with the conventional gate TFT (Perpendicular Channel).

Output conductance of proposed F-shaped gate TFT after bias stress was rarely increased. This experimental result shows that the proposed device has a higher output resistance relatively and a higher floating n+ node voltage than the conventional gate TFTs. Therefore the F-shaped triple gate TFT could prevent unexpected operation in poly-Si analog circuits effectively.

## 4. Conclusion

We have proposed and fabricated the F-shaped triple gate TFT structures consisting of sub-TFTs with different field effective mobilities. And we have verified that the proposed device could improve hot carrier reliability and reduce kink current by minimizing a potential drop across the sub-gate near drain junction.The stable output conductance characteristic is confirmed.

## 5. References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