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Floating gate memory based on ferritin nanodots with high-k gate dielectrics

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1. Introduction

Floating gate memory has been attracting much attention as high-performance and low energy consumption nonvolatile memory. We have developed floating nanodot gate memory by using cage-shaped supramolecular protein, ferritin, and its bio-nanodot (BND).[1] Fabricated BND floating gate memory showed obvious memory operation due to the charge confinement in the embedded BND. In this contribution, we introduced high-k gate dielectric as a tunnel oxide of MOS memory to improve memory performance. The comparison of capacitance-voltage (C-V) characteristics of fabricated BND MOS memory with 5 nm-high-k and 3nm-SiO_2 indicates that superior charge capacity in high-k applied floating gate memory.

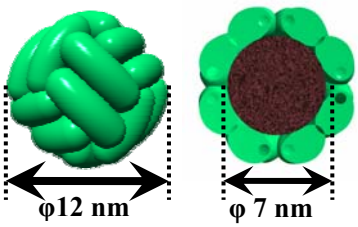

Fig. 1: Ferritin

2. Experimental details

The p-Si (100) substrates with a 3 nm-SiO_2 , 5 nm-Al_2O_3, 5 nm-HfO_2 or 5 nm-HfSiO as a tunnel oxide were cleaned by SPM cleaning and UV/O_3 cleaning to remove hydrocarbon contamination. In order to enhance an adsorption of ferritin, a monolayer of 3-aminopropyl-triethoxysilane (APTES) was formed on top of oxide thin film by vapor deposition. A 0.5 mg/ml of Fe-BND accommodated ferritin solution was applied to the substrates. After ferritin adsorption, outer protein shell was removed by UV/O_3 treatment at 115℃ for 60 min. A 20-nm-thick SiO_2 was deposited by plasma-CVD as control gate oxide. Al electrode was deposited on the SiO_2 layer. Post metallization annnel was acarried out. The MOS capacitor was annealed at 400 ℃ for 1 h in hydrogen gas atmosphere (10 % in N_2) to improve metal contact and reduce Fe core.

3. Result and discussion

Figure 2(a), (b), (c) and (d) shows SEM images of Fe-BNDs on a 3 nm-SiO_2, 5 nm-Al_2O_3, 5 nm-HfO_2 and a 5 nm-HfSiO, respectively. In these cases, we observed high-density adsorption of Fe-BND accommodated ferritin. The average dot density is obtained as 5.9×10^{11}, 6.6×10^{11}, 6.7×10^{11} and 6.5×10^{11} cm^{-2} on SiO_2, Al_2O_3, HfO_2 and HfSiO respectively. These results show high-density Fe-BND absorption was accomplished despite the kind of tunnel dioxide by using APTES.

Figure 3 shows high-frequency C-V characteristics of Co-BND embedded MOS capacitors fabricated with SiO_2, Al_2O_3, HfO_2 and HfSiO as a tunnel oxide.

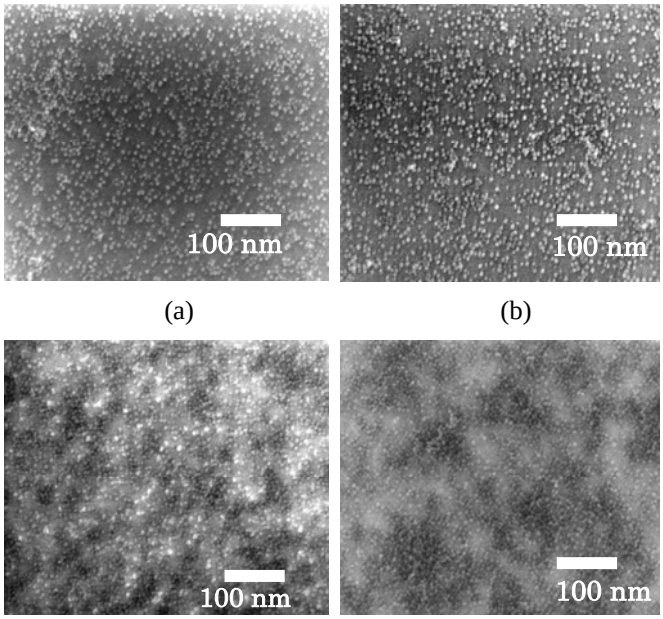

Fig. 2: SEM images of Fe-BNDs on (a) SiO_2, (b) Al_2O_3, (c) HfO_2 and (d) HfSiO.

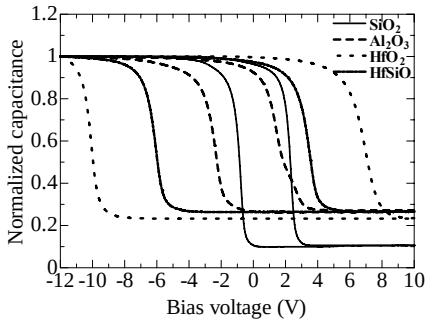

Fig. 3: C-V characteristics of Fe-BND embedded MOS capacitor.

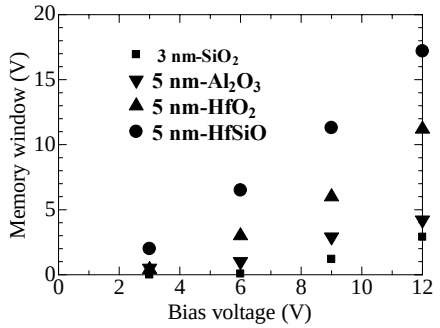

Fig. 4: Memory window

C-V measurements were carried out by changing the DC sweeps of ±12 V at 1 MHz. When SiO_2 and high-k were used, we observed clear anti-clockwise hysteresis in C-V curves. In contrast, hysteresis curve was not observed in case of MOS capacitor without Fe-BND. This indicates that the hysteresis was caused by the charges injected in the embedded Fe-BNDs. Consequently, fabricated MOS memory was successfully operating as nonvolatile memory.

Figure 4 shows memory window size of MOS capacitor. Observed memory window size became larger by increasing DC sweep range. Interestingly, Fe-BND memory fabricated with high-k tunnel oxide showed wider memory window than that fabricated with SiO_2. A physical thickness of 5 nm-high-k is larger than 3 nm-SiO_2, however the effective oxide thickness (EOT) is comparable with or thinner than 3 nm-SiO_2 due to the higher dielectric constant of high-k. Observed wider memory window size is considered due to the difference of current injection mechanism. Electron and hole inject to Fe-BND by direct tunneling when tunnel dioxide is SiO_2. [1] However, electron and hole inject to Fe-BND by FN tunneling when tunnel dioxide is high-k. In addition, electron and hole injected Fe-BND were back-tunneled when tunnel dioxide was SiO_2. [1]

Figure 5 shows charge retention characteristic of MOS capacitor. Charge retention characteristic was improved by using high-k tunnel oxide. This was because effective potential depth of Fe-BND increased when high-k oxide was used as tunnel oxide, as shown in Figure 6.

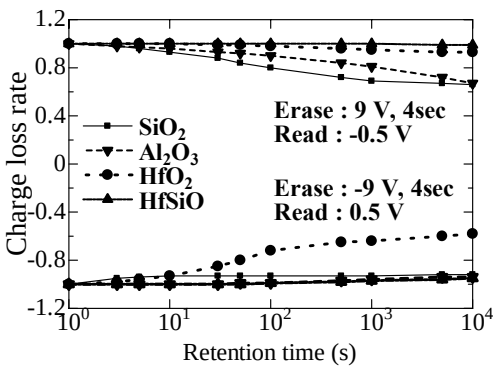

Fig. 5: Charge retention characteristic

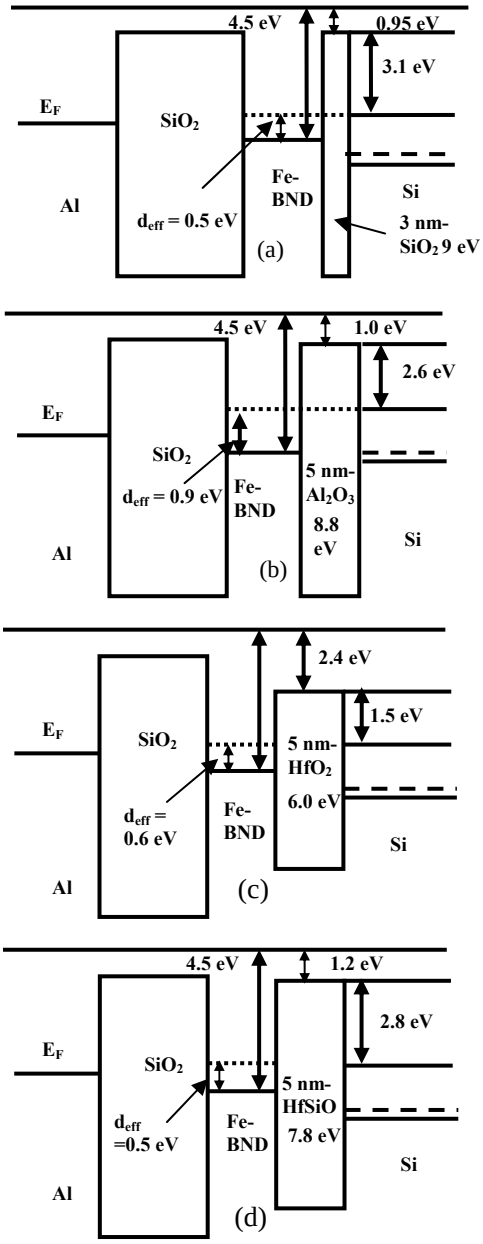

Fig. 6: Band diagram of MOS capacitor with (a) 3 nm-SiO_2 [2], (b) 5 nm-Al_2O_3 [2], (c) 5 nm-HfO_2 [2], (d) 5 nm-HfSiO [3]

4. Summary

We have fabricated floating gate memory device by utilizing ferritin BND and high-k gate dielectric. Fabricated MOS capacitor with high-k tunnel oxide showed good memory characteristics and charge retention characteristic which is better than that of fabricated with SiO_2 tunnel oxide. By using a high-k gate tunnel oxide, further improvement of memory properties were demonstrated.

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References

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