Impact of Quantum Effect on Diffusion Layer Resistance of Si nanowire MOSFETs

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1. Introduction

Si nanowire MOSFET (NWFET) is one of the promising candidates for the future CMOS technology [1][2]. It has been revealed that the width of NWFETs is so narrow that quantum confinement in the channel diffusion regions significantly affects the electrical characteristics. In this work, quantum confinement in the diffusion layers of NWFETs is focused and we clarify the relationship additional resistance due to quantum confinement and the width of NWFETs.

2. Simulation Model and Device Structure

Our simulation is based on a 3D quantum drift-diffusion (QDD) model. In this model, quantum potential based on the density gradient model[3][4] is incorporated into the classical drift-diffusion model. In this study, quantum potential for holes and gate depletion are neglected. Mobility for electrons is constant to examine the effect of the cross-sectional shape on quantum confinement. As depicted below, even if mobility is constant, QDD simulation could reproduce the experiment data.

The diffusion regions next to the channel must also be narrow, even though the contact region is thicker than the channel to reduce the diffusion layer resistance. Since we focus on quantum confinement not only in the channel but also in the diffusion layer, the device structure illustrated in Fig.1 is used. The gate-oxide layer is 1 nm thick, the length of diffusion layer is 0.05um. The doping concentration of p-type substrate is 1x10¹⁷cm⁻³, the doping concentration of n⁺ diffusion layers and n⁻ poly-silicon are 1x10¹⁸cm⁻³. The gate length (L_G) ranges from 100nm to 600nm and the side length (W) ranges from 3nm to 10nm.

After conducting QDD simulations, the diffusion layer resistance and the effective gate length (L eff ) is extracted with the channel resistance method [5].

Figure 2 and 3 are simulation results of rectangular and circular cylinder NWFETs, respectively. Constant mobility is assumed (A) 280cm²/Vs, (B) 900cm²/Vs to reproduce drain currents in inversion region, respectively. The QDD simulation agrees well with both experiment data [6][7]. Mobility is 280cm²/Vs in the following simulation.

3. Simulation Results and Discussion

Figure 4 shows the electron distribution at the middle of the channel (y-z plane) and Fig.5 shows the dependence of threshold voltage (Vth) on W. As the cross-sectional area shrinks, quantum confinement increasingly affects the device characteristics. Quantum confinement become prominent at W below 5nm, because the electron distribution peaks at the center of the channel. Figure 6 shows the dependence of dL on W, where

\[ dL = L_G \cdot \frac{\Delta \rho}{\rho_{cl}}. \]  

Note that dL is negative value. As the cross-sectional area shrinks, there are insufficient electrons in the channel to terminate the electric power line. Hence, the electrons not only in the channel but also in the diffusion layers terminate the electric power line in case of NWFETs. As a result, L eff becomes longer than L_G.

Figure 7 and 8 show the diffusion layer resistance and reisitivity. Shrinkage of the cross-sectional area causes a rise in the diffusion layer resistance. On the other hand, the shrinkage of area results in the decrease of the resistivity in diffusion layers. The decrease of the resistivity is derived from fringe capacitance between gate and diffusion layer. Focusing on the difference between QDD and classical model, quantum confinement induces additional resistance or reisitivity. Figure 9 shows the electron distribution in the diffusion layers. In comparison with the classical model, the electrons are depleted at the Si/SiO₂ interface in QDD model. This depletion effect induces an additional reisitivity. Figure.10 shows \( \Delta \rho / \rho_{cl} \), where

\[ \Delta \rho = \rho_{QDD} - \rho_{cl} \]  

\( \rho_{QDD} \) and \( \rho_{cl} \) are the diffusion layer reisitivity in QDD and classical model. As the cross-sectional area is small, \( \Delta \rho / \rho_{cl} \) monotonically increases and the dependence of \( \Delta \rho / \rho_{cl} \) on the gate overdrive voltage (V ov ) becomes small. In addition, an inflection point appears at W=5nm and this inflection point is independent of V ov . The condition that W is less than 5nm corresponds to the condition that peak of the electron distribution is located at the center of the diffusion layers.

4. Conclusion

We give an extensive study on quantum confinement in the narrow diffusion layer of NWFETs. It is clarified that quantum confinement in the diffusion layers induces the additional reisitivity and that the additional reisitivity extremely increases at W below 5nm. In the sub-10nm technology, the increase rate of the reisitivity due to quantum confinement could reach from 5 to 10 percent.
Fig.1 Cross-sectional view of NWFET.

Fig.2 Simulated $I_D$-$V_G$ characteristics of rectangular NWFET, assuming that mobility is 280cm$^2$/Vs and the flat-band voltage shift is 0V. The inset shows a cross-sectional shape.

Fig.3 Simulated $I_D$-$V_G$ characteristics of circular cylinder NWFET, assuming that mobility is 900cm$^2$/Vs and the flat-band voltage shift is 60mV. The inset shows a cross-sectional shape.

Fig.4 Electron distribution of NWFETs at the middle of the channel (y-z plane). Electron distribution peaks at the center of the channel ($z=0$) at W below 5nm.

Fig.5 $V_{th}$ of NWFETs in QDD and classical model ($L_G=600nm$, $V_{th}=0.05V$).

Fig.6 Dependency of $dL$ on W in QDD and classical model. $dL$ is negative value and $|dL|$ increases as W becomes smaller.

Fig.7 Dependency of diffusion layer resistance on W in QDD and classical model.

Fig.8 Dependency of diffusion layer resistivity on W in QDD and classical model.

Fig.9 Electron distribution at the diffusion layer. Depletion effect at the interface in QDD model induces an additional resistivity.

Fig.10 Dependency of $\Delta \rho/\rho_0$ on W. The increase rate of $\Delta \rho/\rho_0$ is increasing at W below 5nm.

References
[1]: F. L. Yang et al., Symp. on VLSI Technology, p196, 2004
[2]: K. H. Yeo et al., IEDM, p359, 2006
[6]: T. Tezuka et al., IEDM, p887, 2007
[7]: N. Singh et al., IEDM, p547, 2006