Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 1072-1073

H-7-4

Tunneling spectroscopy of germanium quantum-dot in single-hole transistors with self-aligned electrodes

Wei-Ting Lai, Chih-Chun Chen, David M. T. Kuo, and Pei-Wen Li*

National Central University, Dept. of Electrical Engineering
300, Rd. ChungDa, ChungLi, Taoyuan 320, Taiwan, ROC
Phone: +886-3-422-7151-34465 E-mail: pwli@ee.ncu.edu.tw

1. Introduction

Motivation to study a single electron (SE) device is strong in light of its new operating principle, Coulomb blockade (CB) effect, and precise charge sensitivity for single charge/photon detection. The unique charge sensitivity could be applied to single charge or single photon detection, which is crucial for quantum information systems. The carrier transport of a SET can be classified into either a shell-tunneling condition (a QD is empty of a charge) or a shell-filling condition (a QD is occupied with charges). In the shell-tunneling case, electron's Coulomb interactions are suppressed and the corresponding tunneling current spectra directly reveal the 'bare' energy levels of a QD, while the tunneling current spectra become much more complicated in the shell-filling case resulting from the interplay of charging energies and energy levels. Although both physical parameters are crucial not only in the optimization of SETs but also for understanding fundamental physics of miniaturized nanostructure, the charging energies and 'renormalized' energy levels can not be easily resolved from the measured current-voltage (*I-V*) characteristics in the shell-filling case. Furthermore, restrained by the overlay alignment of the existing lithography systems, the fabricated gate electrode generally has to be much larger than the QD size to ensure effective gate manipulation. This will lead to inevitable gate-to-source/drain overlap and severe gate-induced tunneling barrier lowering at the high gate voltage regime. Consequently, the structure of tunneling current smears out and the CB oscillations vanishes, in particular, at high temperature. To solve such a difficulty, smart device structure design and feasible fabrication techniques for effective SETs with self-aligned electrodes must be developed to obtain resolvable CB oscillations with large peak-to-valley ratio (PVCR).

In this paper, we report that high performance Ge SHTs with a single QD simultaneously self-aligned with gate and source/drain (S/D) electrodes could be realized using oxidation of a SiGe-on-insulator 'nanowire' based on FinFET technology. Due to the self-aligned electrodes, the atomic-like characteristics of a Ge QD could be observed from the tunneling current and the coupling strengths between the orbital energies of the QD and S/D electrodes could be revealed from the Coulomb oscillatory current spectra.

2. Experimental and Results

The SHT device fabrication began with a Si buffer (10 nm)/strained $Si_{1-x}Ge_x$ (10 nm) layer and a boron-doped polysilicon (poly-Si) layer (250 nm) deposition on top of an ultrathin silicon-on-insulator substrate. Firstly, a 190 nm nanogap was delineated using electron beam lithography (EBL) and the exposed top poly-Si was etched away 235 nm in thickness using SF_6/C_4F_8 plasma. Then, a poly-Si/SiGe/Si trilayer nanowire (*W/L* = 45 nm/250 nm) connecting S/D electrode pads was formed across the exposed nanogap as shown in Fig. 1(a). Subsequently, a SiO_2/Si_3N_4 spacer (10 nm/65 nm) was deposited and etched using CHF_3/CH_4/Ar plasma. This shrank the exposed SiGe/Si nanogap to 40 nm, ready for subsequent oxidation. After oxidation, a single Ge QD is generated in the core of the oxidized nanowire due to Ge atom segregation and agglomeration, and it weakly couples to adjacent pads via SiO_2 barriers. It is noted that the Si_3N_4 spacer behaves as an oxidation mask retarding oxygen diffusion during the oxidation process, and as a result, no thermal oxidation occurs on the SiGe/Si portion underneath the Si_3N_4 spacer, whereat p^+-S/D electrodes will be formed by dopant diffusion from the top boron-doped poly-Si layer. Subsequently, a boron-doped poly-Si layer was deposited into the delineated gap to form a self-aligned gate electrode with the QD. Finally gate electrode patterning, passivation, contact-hole patterning, metallization, and 400 ^oC forming gas sintering steps were performed to complete device fabrication.

The fabricated Ge SHT is depicted in scanning electron microscopy (SEM) and transmission electron microscopy (TEM) micrographs. It is clearly seen that a single Ge QD forms in the core of a fully oxidized nanowire and weakly couples to the S/D electrodes via 10~15 nm SiO_2 tunneling barriers in Fig. 1(b). Besides, Fig. 1(c) shows that a nanogate electrode self-aligned with the QD has a final gate length of 12 nm, which is nearly comparable to the embedded QD size and much smaller than the nanogap length (40 nm) before oxidation. Such deviation originates from the fact that the Si_3N_4 spacers are pushed inwards during the thermal oxidation process since oxygen atoms diffusing through the SiO_2 spacers cause the adjacent poly-Si to be oxidized. This reduces the gate extension beyond tunneling oxides and suppresses the gate-induced tunneling barrier lowering and parasitic capacitances

significantly. This work provides a simple approach to alleviate the nanofabrication bottleneck and thereby increase design freedom for real SETs.

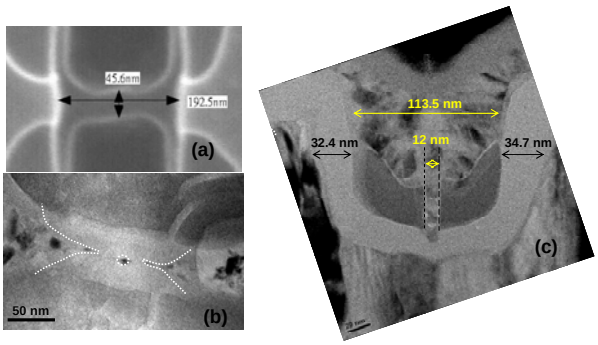

Fig. 1 SEM and TEM images of a Ge-QD SHT. (a) a 190 nm nanogap is delineated across a 45 nm SiGe/Si nanowire, (b) a single Ge QD weakly couples to the S/D electrodes via SiO_2 tunneling barriers, and (c) a self-aligned gate is scaled to 12 nm.

Figure 2 plots the measured tunneling currents and the corresponding differential conductance of a Ge QD SHT as a function of drain voltage at T = 300 K. A Coulomb gap of ~ 27 meV is observed and the threshold voltage of 19 mV at negative drain biases is larger than that (8 mV) at positive drain biases, indicating that the tunneling barrier width between the Ge QD and the source electrode is less than that between the Ge QD and the drain and hence asymmetrical tunneling rates (Γ) are induced in our studied device. We assume that the chemical potential in the QD with respect to that in the source does not move nearly during V_d sweeps because the studied SHT has a relative small gate capacitance due to a thick gate oxide (~70 nm). The gate capacitance (C_g) and junction capacitance, C_d and C_s, are estimated to be 0.15, 0.5, and 1.08 aF, respectively, from the TEM observation. Nearly 70% of V_d is applied to the drain tunneling junction and therefore, the electrostatic conditions for tunneling at the drain side are more prominent, corresponding to the shell-tunneling condition.

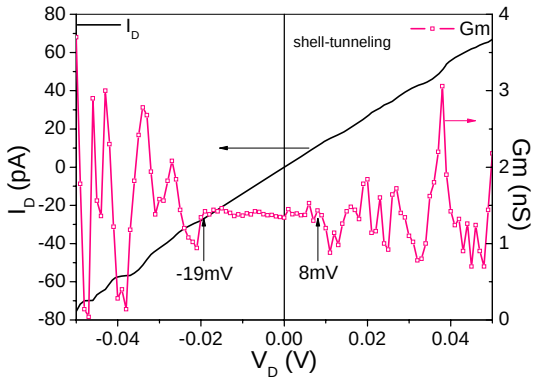

Fig. 2 I_d - V_d of a Ge SHT at T = 300 K.

To further clarify the tunneling current of Fig. 2 arising from the atomic-like characteristics of Ge QDs (discrete energy levels), the tunneling currents with respect to the applied gate voltage with either the drain or the source grounded are studied in Fig. 3. Clear Coulomb oscillatory current peaks with very low leakage current (<10^{-13} A) even at such high gate voltages are observed. This reveals that gate-induced tunneling barrier lowering is effectively suppressed in this Ge SHT, which is benefiting from the self-aligned gate electrode process. The oscillatory peaks in Fig. 3 are attributed to carriers through the resonant channels resulting from the atomic-like characteristics of Ge QDs. In addition, the variation of peak strengths arises from the change of coupling strengths between the orbital energies of the QDs and S/D electrodes. The inhomogenous peak separation arises from one-particle energy levels and Coulomb interactions in the Ge QDs. The quantitative analysis of current spectrum shown in Fig. 3 requires further theoretical works for calculating the hole band structures of Ge QDs and tunneling rate of each orbital, which are determined by the shape, size and location of QDs.

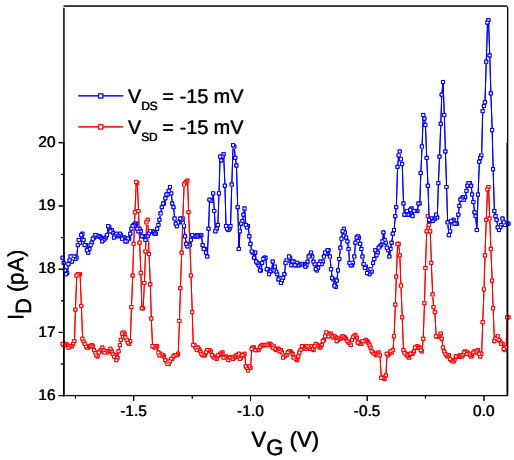

Fig. 3 Tunneling current of a Ge SHT versus gate voltage at V_{ds} = - 15 mV or V_{sd} = - 15 mV at T = 300 K.

3. Conclusions

A single Ge QD forms and is self-aligned with source/drain electrodes via oxynitride tunneling barriers using thermal oxidation of a poly-SiGe-on-Si_3N_4 nanowire. Thereby, a Ge single-hole transistor with self-aligned electrodes is realized and features with large Coulomb-blockade oscillation at room temperature. This work provides a simple approach to overcome the nanofabrication bottleneck and thereby increase the design freedom for SETs.

Acknowledgements

The authors wish to acknowledge the support of National Science Council of Taiwan via the contract No. NSC 96-2120-M-008-001.