H-8-2

Single-Electron Transfer by Controlling the Dopant-Induced Quantum Dot Landscape

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1. Single-electron transfer devices

Single-electron devices (SEDs) have the capability of operating with individual charges, which makes them promising candidates for future electronics.¹ Among SEDs, an important category is formed by single-electron transfer devices, able to transfer elementary charges synchronized with external voltage pulses. Some design schemes have been already proposed based on precisely defined quantum dot (QD) arrays. The original single-electron turnstiles and pumps transfer electrons one-by-one during every cycle of one or, respectively, several ac gate voltages applied simultaneously to a 1D array of metallic QDs. Achieving such capabilities in semiconductor devices is essential for practical applications. In this direction, single-dot SEDs have been demonstrated to work as turnstiles and pumps by an appropriate control of the dot-lead coupling by ac-gates.²

We approach the issue of single-electron transfer operation in silicon-based devices from a different angle: utilizing dopant-induced OD arrays. We have recently demonstrated that phosphorus-doped-nanowire SOI-FETs exhibit single-electron transfer features (i.e., ef plateaus in the I_{SD} - V_{SD} curves measured under ac-gate operation).⁵ This finding is supported by simulations which indicate that inhomogeneous QD arrays (such as introduced by randomly-distributed promote ionized dopants) single-electron transfer operation.⁶ The success rate of single-electron transfer obtained from statistical simulations depends both on the number of dots in the system and on the parameter dispersion. It becomes necessary now to find methods of adjusting the QD structure in doped nanowires to meet the requirements for single-electron transfer. In this work, we show how the top and back gates can be used to favorably modify the dopant-induced QD landscape.

2. Dopant-induced quantum dot arrays

Figure 1(a) shows the bare dopant-induced potential landscape calculated for a random dopant arrangement. As expected, the potential profile is inhomogeneous due to the non-uniform distribution of dopants, leading to creation of inhomogeneous QD arrays.

The structure of the QD arrays can be modified by adjusting the Fermi level relative to the modulated potential (see Fig. 1(b)). It can be noticed that the number of dots, as well as the relative sizes of the dots and tunnel barriers, can be thus changed. Therefore, we suggest that gate voltage adjustment of the actual dopant-induced potential landscape can give us the capability of inserting or removing single dots into/from the array. Adding another dot into the system introduces new stable charge states that can be utilized for conveying one electron from one end of the QD array to the other, under appropriate biasing conditions. We will demonstrate this capability in the next section.

3. Single-electron transfer in doped-nanowire FETs – experimental results

We have measured the electrical characteristics of doped-nanowire SOI-FETs, as shown schematically in Fig. 2. Dc source-drain current (I_{SD}) - top gate voltage (V_G) characteristics taken for a back gate voltage of 0 V at 16 K are shown in Fig. 3. The oscillations of the current are a clear signature of charge transport based on the Coulomb blockade effect in QDs. Furthermore, peak splitting of the Coulomb oscillations indicates the formation of a QD array within the device channel. For the purpose of achieving single-electron transfer, the device should operate very close to the threshold, where the channel is almost completely depleted of carriers. Therefore, we focus on this region of V_G and investigate how back gate voltage affects the device behavior.

Figure 4 shows comparatively two stability diagrams measured for the same device. The difference between these two measurements is the back gate voltage: $V_{BG}=0$ V [Fig. 4(a)] and V_{BG} =-5 V [Fig. 4(b)]. For both situations, diamond-shaped regions where current is essentially zero can be observed. There are, however, some important structural changes, indicated by the guides for the eyes: a new stable region emerges close to the pre-existing ones when V_{BG} is changed from 0 V to -5 V. We suggest that this may be due to the introduction of a new dot into the system by V_{BG} adjustment (this can be also regarded as the introduction of another QD in the electron conduction path). The presence of the newly-formed stable region creates a strong overlap (hysteresis) with the neighboring regions. It should be expected that a top gate voltage swing crossing this hysteresis area (as illustrated in Fig. 4(b)) can make the system transfer a single charge from one end to the other of the array (similar to typical turnstile operation). The transfer electron can be inserted in the array from source when the gate voltage exits the left-hand stable region (at point 1) and then it can be extracted through the other arm of the array when gate voltage returns by exiting the newly-found diamond region (at point 2).

In order to prove this assumption, we measured the ac-gate behavior of this system by setting the gate voltage offset V_{G0} inside the hysteresis area and applying a small-amplitude (50 mV) pulse around this value. The characteristics are given in Fig. 5 for dc and ac-gate operation (for V_{BG} =0 V and -5 V) for the same value of the dc-gate voltage offset (V_{G0} =-380 mV). The ac-gate characteristics measured for V_{BG} =-5 V show a current plateau region in V_d aligned around *ef* level for *f*=1 MHz operation frequency. This is an evidence of the fact that, under the above-mentioned conditions, the dopant-induced QD array is able to transfer electrons one-by-one between source and drain electrodes. Hence, adjustment of top and back gates offers the possibility of optimizing the QD structure for single-electron transfer operation.

Conclusions

Discrete distribution of dopants in nanometer scale nanowires leads to the formation of inhomogeneous QD arrays. We suggest a simple method of controlling the dopant-induced QD landscape in order to achieve optimal conditions for single-electron transfer operation.

This work was partly supported by MEXT KAKENHI (18063010 and 16106006). We thank T. Mizuno and D. Nagata for support during the experiment.



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Fig. 2 Schematic device structure (wire length=100 nm, wire thickness<10 nm, gate oxide~10 nm).



Fig. 4 Stability diagrams measured for different back gate voltages: (a) $V_{BG}=0$ V; (b) $V_{BG}=-5$ V. A new diamond-shaped stable region (and a new hysteresis in V_G - V_{SD} plane) appears by applying negative V_{BG} .

Fig. 3 Source-drain current (I_{SD}) as a function of top gate voltage (V_G) measured at 16 K. Coulomb oscillations can be observed as an evidence of the presence of a multi-dot array in the channel.



Fig. 5 Source-drain current vs. source-drain bias curves measured by setting V_G in the area indicated in Fig. 4. The case of ac-gate operation with 1 MHz frequency and back gate voltage V_{BG} =-5 V exhibits a plateau aligned at $e \times f$ current level (single-electron transfer operation).