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Silicon based Technology for Single Dopant Orbital Transistor

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Introduction

Standard CMOS technology is reaching some limits with next technological nodes. Alternative architectures are proposed in order to continue scaling down to 11 nm node [1-5]. Nevertheless variability issue, caused by process dispersion, becomes critical, even for 45 nm node. And solutions, like designing circuits at the worst case rules, lead to an increase in power consumption.

One major issue for variability is channel doping. Efforts for atomic control of dopants are pursued worldwide [6-8] and the detection of single dopant is possible by transport [9, 20] or charge sensing methods [10]. Atomic control will improve FET performance for devices above the 45 nm node [6] but will also allow new operating modes for more aggressive devices, based on the convergence between the FET and the SET [11].

By analogy with transport through atomic orbitals from bottom-up approaches (break junctions [12], molecular transport [21]), the European project AFSID (Atomic Functionalities on Silicon Device) will consider a top-down technique. It combines a competitive silicon technology with single ion implantation to compare switches based on single dopant atomic orbitals and those based on artificial silicon atoms.

1. Single atomic orbital transistors (SAT)

The source drain current of devices containing numerous dopants could be dominated by resonant transport through a single dopant [7]. The advanced CMOS developed within the microelectronics platforms permits to reach the limit where in average one single dopant is implanted below the gate (see fig 1). The top gate which protects the channel during source-drain implantation allows the transmission through the single dopant to be tuned. A further step could be accomplished by detecting in-situ the implantation of a single dopant thanks to the IBIC technique [8] or thanks to the modification of the drain current [7]. Although variability in the 10nm range on the dopant position is left after implantation, the precise location of the dopant could be determined afterwards by transport spectroscopy measurements performed at low temperature. The resulting SAT will be a switch of very good electrostatic intregrity, and low power consumption.

2. Silicon artificial atoms (ultimate MOS-SET)

Recent works show that controllable Silicon SET using a single gate, self aligned spacers and doping modulation have size in the 30 nm range and charging energy of few meV [13]. Recent advances in silicon technology also suggest that such devices can be made even smaller, forming artificial atoms from undoped silicon channel. Because of the proximity in terms of architecture and design for the SAT and the ultimate MOS-SET (fig 2)- the main difference relying in the channel and LDD doping level (see figures 3 and 4)- the comparison of their performances will be very fruitful to evaluate the advantages of silicon SET, resonant tunnelling devices and FET as electrical switches.

3. Silicon based technology.

Transistor fabrication

The starting substrate is SOI. After having thinned down the silicon film to the desired value, we perform channel implantation. A MESA isolation is used to define active area. Then 4 nm gate oxide is grown and N+ doped polysilicon is deposited as a gate metal. Nitride spacer is realized and its thickness can be tuned leading to either overlapped or underlapped device. Then raised S/D are performed. Next step is HDD implantation, and we end the S/D module definition by Ni silicide. Standard encapsulation finishes the fabrication of the device.

Channel implantation

For the single atomic orbital transistor, the objective is to obtain a single dopant in the silicon wire defining the channel. Two solutions are proposed.

First, a dose implant of 1E12 at.cm^{-2} corresponds to an average of a single atom per 10*10 nm², which is our objective in terms of channel dimension. Energy is then adapted in function of the thickness of the channel. Fig 5 & Fig 6 shows doping profiles in Si, based on CTRIM simulation for two species: Se and P, shallow impurity and deeper one (for higher temperature functionality), through 2 nm of SiO_2. For each ion, optimal energy is chosen so that R_p is in the middle of the channel and the maximum dose corresponds to an average of an atom in a box of 10*10*10 nm^3(1E18 at.cm^{-3}). Then measurements and statistical studies will enable localisation of dopants in Si layer thanks to a large amount of samples fabricated in LETI clean room.

Second technique will use a skill developed by the University of Melbourne and based on IBIC (Ion Beam Induced Charge) [8]. Indeed a Phosphorus ion implanted at 14 keV leads to the creation of about 1000 electron holes pairs. So the technique consists in detecting the formation of these pairs by collecting electrons in the drain of the device thanks to a transverse field (fig 7). Alternatively implantation could be detected by induced variation of channel conductance in our very small structures.

Lithographic performance

On one side, Si structures in the 10 nm range are required for quantization energy in the 10 meV regime and coulomb charging energies around 50 meV, above k_BT=25 meV at room temperature. On the other side, to achieve complex functionalities SET and SAT need to be efficiently capacitively coupled to each others [14-15]. Thus lithography is asked at the same time to have high resolution in terms of minimal size and spacing and good overlay performance.

Usual trimming process is not adapted at this aim, because reducing the size of patterns it also increases the spacing between them. Therefore lithographic process is critical.

High resolution Gaussian electron beam lithographic tool will enable this ultimate resolution. Combined with NEB35 resist [16], 20 nm line width is obtained (fig 8) and spacing down to 40 nm (fig 9). Alignment strategy is also well controlled. It ensures precision of alignment between two levels below 10 nm (fig 10).

Thin film process

The most ultimate resolution must be obtained along x and y axis, but also in the thickness of the devices. So we take advantage of the experience of the LETI in processing thin films devices [17]. It is helped by successful epitaxial process on thin films [18], below 10 nm. It enables the salicidation of S/D and the optimization of the resistance.

Conclusion

The combination of CMOS platform facilities with controlled single dopant implantation enables fabrication of switches based on tunable single dopant orbital. SET-FET convergence will be tested by comparing single dopant FET and undoped SET of the same size.

Aknowledgements

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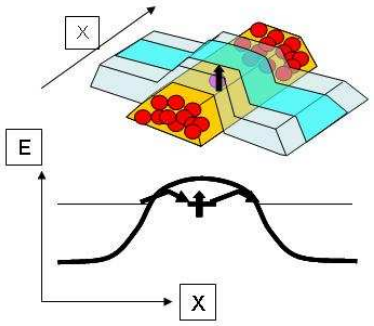


.Fig 1 : Schematic view of an atomic orbital transistor and its potential profile along the wire a single dopant is localized in the channel

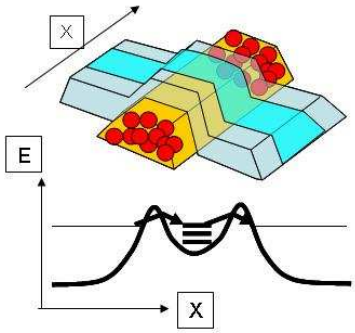


Fig 2 : Schematic view of an ultimate MOS-SET and its potential along the wire. The spacers will mask the island and barrier region during source/drain implantation [13] (no channel and LDD implantation)

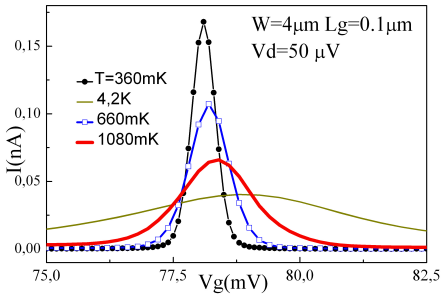


Fig 3 : Resonant drain current versus gate voltage in the subthreshold regime of a MOSFET. At low temperature the drain current is dominated by resonant tunnelling through centered dopants in wide [19], as in narrow [9] channels.

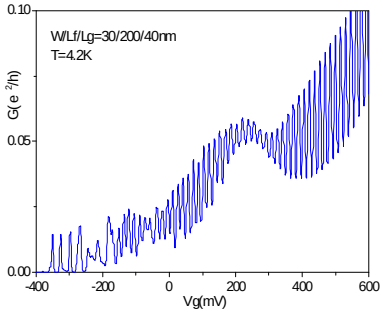
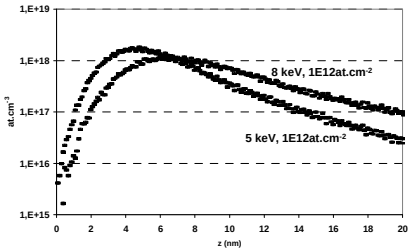


Fig 4 Periodic Coulomb Blockade Oscillation obtained at T=4.2K in a ultimate MOS-SET [13]



*.Fig 5 : Selenium doping profiles in Si layer. Optimal energy for 10 nm is 5 keV. For thicker film around 20 nm, 8 keV shows Rp in the middle of the film. Rp concentration is 1E18 at.cm-3, corresponding to 1 atom in a cube of 10*10*10 nm^3 .*

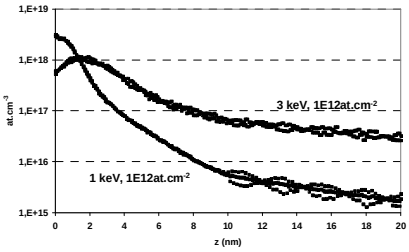
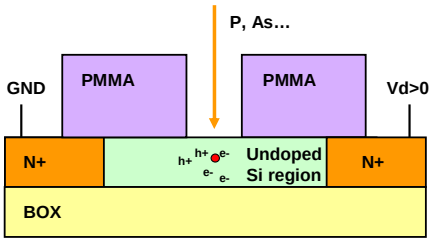


*Fig 6 : Phosphorus doping profiles in Si layer. Optimal energy for 10 nm is 1 keV. For thicker film around 20 nm, 3 keV shows Rp in the middle of the film. Rp concentration is 1E18 at.cm-3, corresponding to 1 atom in a cube of 10*10*10 nm^3 .*



.Fig 7: Single dopant implantation through a mask in a thin film. The detection can either be performed via IBIC (large Vd bias) or by channel conductance variation.

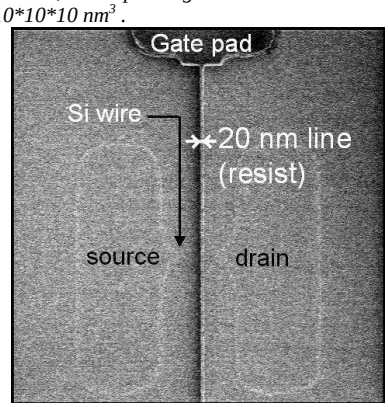


Fig 8:20 nm line obtained thanks to Gaussian beam and NEB35 resist.

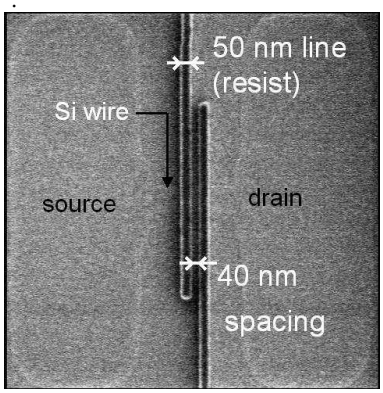


Fig 9: Two 50 nm lines with 40 nm spacing are obtained and enable very accurate coupling between dots

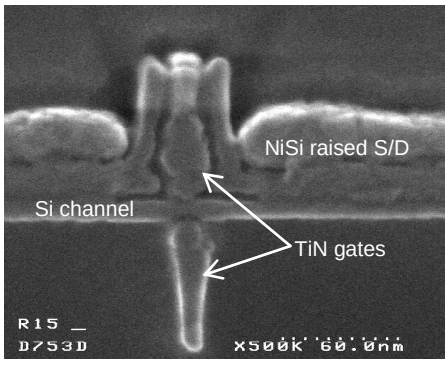


Fig:10: Double Gate MOS transistor fabricated thanks to two gate successive lithographies. The targeted positions of the two gates were reached within a 10 nm accuracy.