Dopant Freeze-out and Potential Fluctuations Observed by Low Temperature Kelvin Probe Force Microscope

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Motivation

Single Electron Devices (SEDs) are very promising for fabrication of future Ultra-Large Scale Integrated (ULSI) circuits, sensors, memories or metrological tools due to their ultimate properties of manipulating elementary charge. The possibility of significant reduction of parameters such as device size or power consumption makes SEDs being widely investigated at present. One of the approaches to achieve single electron transfer is by creating quantum dot (QD) arrays in the Si nanowire utilizing natural potential fluctuations caused by ionized dopant atoms¹. Thus it is crucial to monitor the potential distribution inside doped nanowires.

So far, none of the proposed methods^{2,3} are capable of "looking" beyond several topmost layers . Low Temperature Kelvin Probe Force Microscope (LT-KFM) seems to be an appropriate tool for this purpose due to its high sensitivity to charges placed deeper in the device structure. Therefore we believe that KFM may be utilized to sensitively detect dopant induced potential fluctuations and for that goal we have investigated the surface potential of MOSFETs in the wide range of temperatures. We found direct evidence of the dopant freeze-out in nanodevice channel. Moreover we present the observation of potential fluctuations which may appear due to discrete distribution of dopants in the channel.

Dopant freeze-out

For the purpose of this research several samples have been fabricated with the structure shown in Fig. 1. For all the samples top Si region was doped with phosphorus (P: $5x10^{17}$ cm⁻³), while BOX layer thickness was 150 nm. The substrate was heavily doped with boron (B: $2x10^{18}$ - $3x10^{19}$ cm⁻³). During the measurements, the top surface of few devices was investigated by KFM at different temperatures (13K, 38K, 70K and 300K). Both source and drain were grounded, while back gate voltage (V_g) was swept from -4 V to 4 V at each temperature. The line scans of the potential of the channel and BOX surfaces were taken for measured devices.

In Fig. 2 and Fig. 3, we observe the topography profiles (dot line) and corresponding electronic potential profiles (solid lines) taken at 300K and at 14K respectively. It is noticeable that the BOX (SiO₂) surface potential is always changing according to applied Vg. It is understandable since sample substrate is a p^+ heavily doped Si and thus it is conductive even at low temperatures. Far from the channel BOX layer is perfectly floating therefore its surface potential should reflect the potential of the underneath p^+ -Si substrate (which is equal to applied Vg). Fig. 2 and Fig. 3 show however -2V shift of the BOX surface potential. We ascribe this shift to surface charging since BOX thickness is around 150nm and no Vg influence on charge distribution

can be observed. According to [4] if the insulator (SiO₂) thickness is greater than tunneling distance (~2-3 nm) oxide surface may retrain charges for a long time. Interface trapped charges on the other hand should redistribute due to Fermi level or band banding change⁵. Therefore results seem to reflect surface charges rather than interface traps.

On the contrary to the BOX, channel surface potential observed in Fig. 2 and Fig. 3 depends on the Vg only at low temperature and remains fixed around 1V at room temperature. In Fig. 4 we can see the difference of channel surface potential for Vg=-4V and Vg=+4V at different temperatures. It is visible that with decreasing the temperature the channel surface potential dispersion due to applied Vg is rising. We believe this tendency is indicating dopant freeze-out in the channel. As shown in Fig. 5 the number of free carriers in Si strongly depends on the temperature⁶. In room temperature the channel is fully conductive, therefore its surface potential remains fixed close to ground level (Fig. 6a). In low temperature on the other hand, as the number of ionized dopants and thus number of free carriers decrease, channel becomes partially floating. As a consequence its surface potential starts to be modulated by applied Vg (Fig. 6b).

Above results prove high capabilities of LT-KFM used for our research. Not only dopant freeze-out in the channel can be directly observed but also background charges may be detected. Both issues are of great importance in case of SEDs and therefore further investigation is needed.

Dopant induced potential fluctuations

In Fig. 7 we can see the potential profiles taken at 70K. For this device characteristic potential fluctuations appeared in the channel region (Fig. 8b). We believe that these features are induced by ionized dopant atoms. We exclude interface trapped charges since similar potential fluctuations cannot be observed in the BOX region. Also surface charging is unlike since results shows strong Vg dependence. In Fig. 8 we can compare the simple estimation of the dopant induced potential landscape for random dopant distribution (Fig. 8a) with measurement results (Fig. 8b). The profiles obtained from KFM are matching with our expectations of dopant induced potential fluctuations. Also 200mV amplitude is reasonable. We expect that after further optimization of measurement conditions and device structure we will be able to resolve single dopant effects.

Conclusions

We have shown the high capabilities of LT-KFM. Using this microscope we can directly observe freeze-out of dopant atoms in the MOSFET channel under operation. Moreover we show that LT-KFM may be utilized to detect dopant atoms in the MOSFET channel.

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Fig. 2 Vg dependence of surface potential taken at 300K



Fig. 4 The temperature dependence of the channel surface potential difference for Vg=+4V and Vg=-4V











Intri

regi

 $=N_D$



Fig. 6 Potential profile along the channel for various Vg at a) room temperature; b) low temperature



200

10

100 200 300 400 500 600

region

 $T(\mathbf{K})$

Fig. 5 Electron density as a function