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Fabrication and characterization of CdF_2/CaF_2 resonant tunneling floating gate metal-oxide-semiconductor field effect transistor structures

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1. Introduction

A CdF_2/CaF_2 heterostructure is an attractive candidate for quantum applications on Si substrates, such as resonant tunneling diodes (RTDs)[1] and coulomb blockade devices, because of the large conduction band discontinuity (ΔE_C~2.9eV) at the heterointerface [2] and small lattice mismatch with silicon. Due to the large ΔE_C, leakage current is expected to be suppressed in low level even at room temperature and moreover, voltage for tunneling transport can be reduced by utilizing multi-quantum-well tunneling scheme such as resonant tunneling or sequential tunneling with appropriate design of quantum-well layer thickness sequences. Up to now, we have demonstrated large peak-to-valley current ratio (PVCR) of CdF_2/CaF_2 RTDs larger than 10^5 at RT [3], which confirmed advantage of the large ΔE_C heterostructure material systems.

In this paper, we have proposed and demonstrated metal-oxide-semiconductor field effect transistor (MOSFET) integrated structures with CdF_2/CaF_2 resonant tunneling floating gate.

2. Structure

Schematic device structures are shown in Fig.1(a). MOSFET structures are fabricated on p-type (~10^{16}cm^{-3}) silicon-on-insulator (SOI) with 200 nm in thickness. Gate length is 5 μm and width is 50 μm with n-type (10^{16}cm^{-2}) source and drain region. CdF_2/CaF_2 triple barrier resonant tunneling structures are grown in hole array of 100 nm in diameter with 250 nm-interval formed in 10 nm-thick SiO_2 gate oxide region as shown in Fig.1(b). Limitation of crystal growth region in nano-area holes significantly enhance high-quality epitaxial growth of CdF_2/CaF_2 heterostructures especially on Si(100)[4,5]. Au/Al is used as gate electrode.

Resonant tunneling floating gate regime enable reduction of gate voltage for charge injection and ejection. Electrons are injected from gate metal (Al) into CdF_2 quantum-well through resonant tunneling and trapped due to energy relaxation by scattering. Trapped carriers are ejected by reverse bias through tunneling. In the result, write/erase voltage can be reduced by resonant tunneling with keeping long retention time under off-resonance bias condition.

3. Fabrication

SiO_2 hole arrays for gate RTDs were pattered by electron-beam lithography and wet etching using HF.

The protective oxide layer (in the growth region) was removed in an ultrahigh-vacuum (<10^{-7}Pa) chamber by thermal heating with a Si flux at 700°C. Subsequently, a 1.6-nm-thick CaF_2 layer was grown at 120°C and thermally annealed at 500°C for 10 min in a molecular beam epitaxy (MBE) chamber for solid phase epitaxy. Subsequently, a 4.3-nm-thick CdF_2 quantum-well layer, 1.6-nm-thick CaF_2 layer, 1.6-nm-thick CdF_2 quantum-well layer and 1.6-nm-thick CaF_2 top barrier layer was grown at 80°C. Finally, Al/Au electrodes were formed by lift-off.

4. Results and discussions

In the measurement of I_D-V_D curve shown in Fig. 2, threshold voltage shift was clearly observed in the variation of drain current more than 50%, corresponding to charged state and non-charged state of RTD gate structures. Figure 3 shows I_G-V_D curve, which clearly shows electron injection gate current at V_D = 15V and discharge current at around V_D = 0 V, respectively. These behaviors are consistent with negative differential resistance characteristics of RTD structures of the same layer structures. From the theoretical analysis of potential distribution around the channel, charge density of RTD region was evaluated.

5. Conclusion

We have fabricated MOSFET structures with CdF_2/CaF_2 triple barrier resonant tunneling floating gate and demonstrated fundamental memory operation by threshold voltage shift corresponding charged and discharged state of CdF_2/CaF_2 heterostructures. These results are mile stone for device application of Fluorite based heterostructures integrated with Si-MOSFET technologies.

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Fig. 1

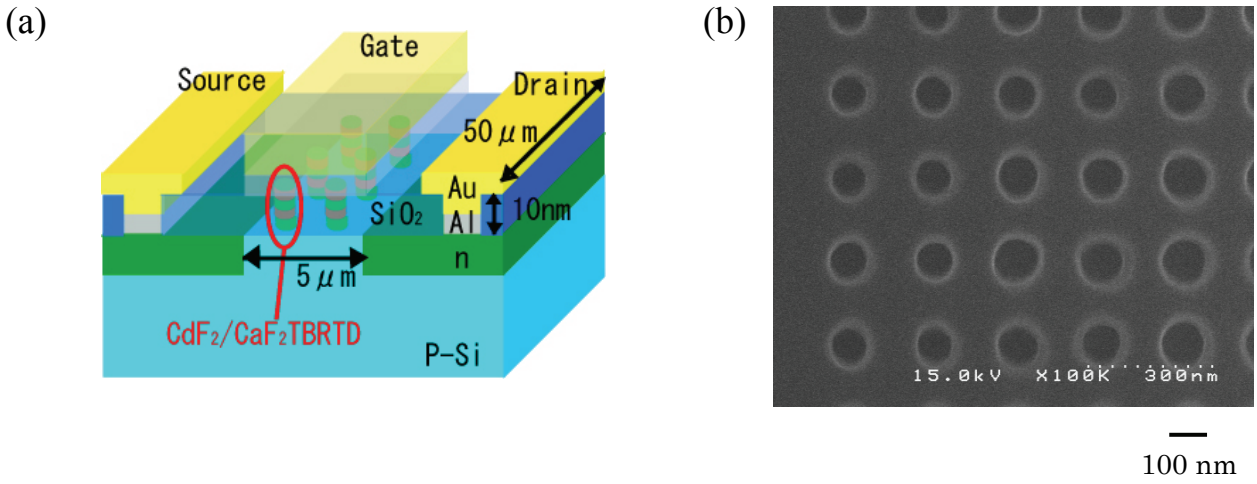

Fig. 2

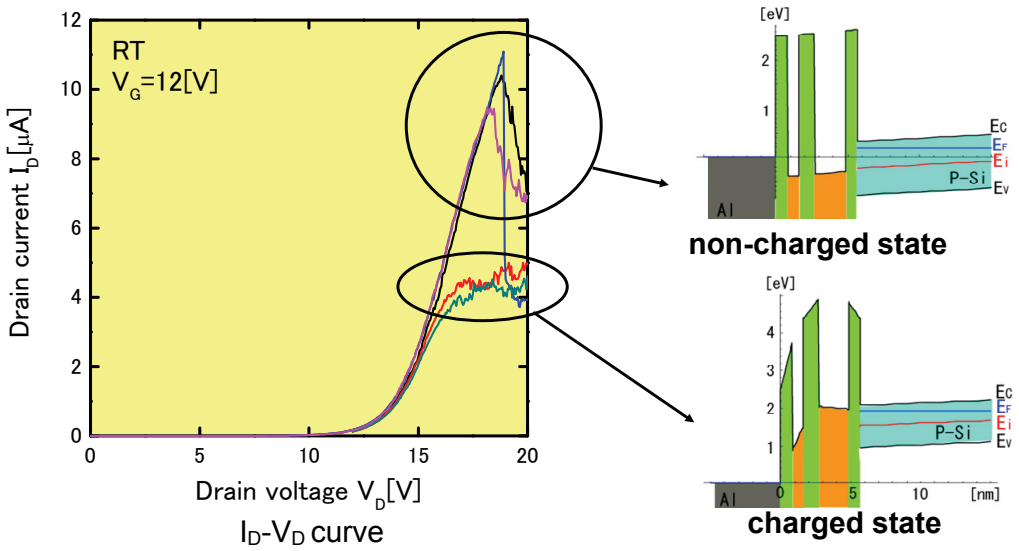

Fig. 3