Enhancement of Carrier Mobility by Controlling the Initial Pentacene Growth Modes on SiO₂ Dielectric Layer

Chao JIANG¹, Qiong QI, Aifang YU

¹National Center for Nanoscience and Technology No. 11, Beiyitiao Zhongguancun Beijing 100190, China Phone: +86-10-8254-5563 E-mail: jiangch@nanoctr.cn

1. Introduction

To realize the reliable device performance in the realistic applications, organic Thin-Film Transistor (OTFT) needs high carrier mobility and large saturation current to be applied to the fast switch and feasible driving circuits. For this purpose, lots of approaches have been utilized to improve Penetace ($C_{22}H_{14}$)-based transistor's mobility, such as improving the surface roughness of the dielectric materials[1], modification of the dielectric surface by self-assembled monolayer[2], etc.

In recent, several research groups report that a continuous complete and less boundary defects single monolayer of pentacene is virtually essential to achieve high mobility and large driving current, because grain boundaries strongly limit the mobility and the charge transport in pentacene films[3]. In this letter, we focus on the control of initial growth behavior of pentacene to be layer-by-layer two-dimensional growth mode on the first monolayer and by this approach we gain the best mobility for pentacene OTFT on bared SiO₂/Si substrate. The mobility in saturation region can be high to reach 1cm²/vs and the saturated current to be 300 μ A under the V_{ds} = -40V, indicative of a promising novel pentacene TFT fabrication approach for realistic device application.

2. Experimental

The pentacene TFTs were fabricated on heavily doped n-type (001) silicon wafer having a 250 nm SiO₂ layer as a dielectric layer grown by a conventional wet thermal oxidization process. The typical root mean square (RMS) surface roughness for the SiO₂ determined by atomic force microscopy (AFM) is 0.3 nm. The substrates were ultrasonically cleaned by three various approaches: method one with the ammonia solution $NH_4OH:H_2O = 1:6$ for 10 minutes, then deionized water for 10 minutes; method two with the $NH_4OH:H_2O_2:H_2O = 1:1:5$ (APM) and HCl:H2O2=1:1:6 (HPM) for 10 minutes, respectively and then deionized water for 10 minutes; while method three with only organic cleaning using acetone, ethanol and deionized water, each for 20 minutes, respectively. All cleaning methods have not further introduced substrate roughness via a later AFM investigation.

50 nm Pentacene (purity 97% from Aldrich Co.) films calibrated by a quartz oscillator analyzer were deposited on the substrates by a commercial thermal evaporator Auto-306 (BOC-Edwards Co.) deposition system equipped with an independent K-cell of pentacene in addition to four metal evaporator cells. During deposition, the back pressure reached 7×10^{-5} Pa with deposition rate 0.02 nm/s under the

room temperature. Finally, 50nm-thick Au source-drain electrodes were deposited through a shadow mask onto the 50nm Pentacene film at a rate of 0.4nm/s to finish the top-contact TFTs fabrication with the conductance channel length and width 50 μ m and 2000 μ m, respectively. The morphology of the pentacene film deposited at various thicknesses on these dielectrics was characterized by a Nanoscope III (Veeco Co.) AFM using tapping mode. The contact angle was measured using distilled water and the transfer curve of TFT was characterized using a Kethley-4200 semiconductor analyzer.

3. Results and Discussion

Morphology and Ordering

Figure 1 shows the comparison of the morphology of 50 nm pentacene grown on SiO₂ dielectric treated with cleaning method-one and three. On the dielectric treated with ammonia (Fig. 1a), pentacene grains exhibit dendritic structure with average grain size of 800nm in contrast to small grains with average grain size of 200nm as shown in Fig.1b whose dielectric substrate was cleaned by the organic cleaning. Nevertheless, the electric transport properties for the two TFTs are of drastic difference and a factor of five in between in the carrier mobility exists. The rocking curve by X-ray diffraction for these two 50nm thick pentacene films showing a pure thin-film phase characterized with an interplanar spacing of 1.55nm is recorded for a comparison. The intensity of peak is significantly stronger on gate dielectrics with cleaning method-one than that on the gate dielectrics cleaned with organic solvent, indicative of much better crystal quality and more arrangement ordering of pentacene molecules in the former than the later.



Fig. 1 AFM images of 50 nm thick pentacene deposited on SiO2 cleaned by (a) ammonia solution, and (b) organic solvent.

Device Performance

The output I_d -V_{ds} characteristics under the various gate biases for TFTs with different surface treatments are shown in Figure 2. Saturation behavior of drain current at high drain-source voltage (V_{ds}) was observed for all devices and its values are markedly dependent on the surface treatment procedures. The biggest maximum saturation currents 303 μ A was obtained for the OTFTs based on ammonia treatment when the drain voltage was swept at a constant gate-source voltage. The carrier mobility of the TFTs was calculated in saturation regime from a plot of the square root of the drain current versus V_{GS} by fitting the data to the equation (1). Table 1 also summarizes the results for V_T, V_{to}, V_{to}, I_{on}/I_{off}, subthreshold swing S, and calculated mobility.

$$I_{DS} = \frac{W}{2L} C_{OX} \mu (V_{GS} - V_T)^2$$
 (1)

Transport Mechanism by Investigating the Initial Growth

Figure 3 shows the AFM images of pentacene film grown on various treated SiO_2 surfaces with a nominal thickness of 0.5 ML. On the surface treated with ammonia (Fig.3c), pentacene has homogeneous nucleation, and form flat islands having the lobular shapes and smooth borders with a typical monolayer height of approximately 1.5nm which was ever observed under hyperthermal molecular beam deposition by a molecular energy higher than 6.4eV. On the contrary, the pentacene islands are located disorderly on the substrate with different size, height, and shape on the surface treated with acetone and ethanol (Fig. 3a).

The high carrier conductance we observed in Fig.2 is probably attributed to the perfect healed grain boundaries as confirmed in higher coverage pentacene film[4]. In this layer-island S-K-like grown mode, the strength of the molecule-molecule interaction is weaker than molecule-substrate interaction, and the first molecules have a tendency to form a flat monolayer on the substrate. With the increasing of deposition amount, the pentacene occupied almost all the first layer. Thus molecule-substrate interaction became weaker and many two-dimensional islands were observed with single monolayer step edges. By this growth mode, we can easily obtain a flat and homogenous continuous pentacene layer.

4. Conclusion

We have investigated the impacts of cleaning method on structure, morphology, as well as TFT device performance of pentacene film. Pentacene grown on SiO₂ with surface cleaned by acetone-ethanol was dominated by three-dimensional mode. Whereas, when the surface cleaned with ammonia, S-K mode was occurred. The electrical characteristics of Pentacene-TFTs especially mobility, grain size and the ordering of pentacene molecules based on SiO₂ cleaned with ammonia are significantly improved. With this surface cleaning treatment, the mobility of pentacene-OTFT reaches 1.00 cm²V⁻¹s⁻¹, and the subthreshold swing S decreases to 0.7 Vdecade⁻¹, thus OFET performance is determined by the



quality of first few pentacene monolayers, especially the first monolayer.

Fig. 2 Electrical-transfer characteristics of TFTs with three different surface treatments of SiO_2 cleaned by (I) ammonia; (II) APM and HPM; (III) acetone and ethanol.



Fig. 3 $3\mu x^3\mu AFM$ image of 0.5 monolayer thick pentacene deposited on SiO₂ cleaned by (a) acetone and ethanol; (b) APM and HPM; (c) ammonia.

 Table I
 TFT properties for different surface cleaning treatments.

Surface	Mobility	VT	I_{on}/I_{off}	Θ
treatment	$[cm^2V^{-1}s^{-1}]$			[degree]
Method-	1.0	-1.1	1.1E6	51
one				
Method-	0.72	-1.0	5.1E4	50
two				
Method-	0.21	0.9	3.2E3	62
three				

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