

## Low Voltage and Small Subthreshold Swing HfLaO/Pentacene Organic TFTs

M. F. Chang<sup>a</sup>, P. T. Lee<sup>a</sup> and Albert Chin<sup>b,c</sup>

<sup>a</sup>Dept. of Photonic and Inst. of Electro-Optical Eng., National Chiao-Tung University, Hsinchu, Taiwan, ROC

<sup>b</sup>Dept. of Electronics Eng., National Chiao-Tung University, Hsinchu, Taiwan, ROC

<sup>c</sup>Nano-Electronics Consortium of Taiwan, ROC E-mail: [albert\\_achin@hotmail.com](mailto:albert_achin@hotmail.com)

### 1. Introduction

Pentacene based organic thin-film transistors (OTFTs) [1]-[2] have attracted much attention beyond poly-Si TFTs [3]-[5] for low-cost light-weight displays and flexible ICs. However, the fundamental challenges for OTFTs are the high threshold voltage ( $V_T$ ) and poor subthreshold swing (SS). The OTFTs are generally operated at high voltage of >15 V that is not suitable for low voltage and low power ICs. The poor SS slows down the switching speed of inverters used in logic circuits. In this paper, we have addressed these issues by first exam the  $V_T$  relation:

$$V_T = \phi_{ms} - Q_{tot}/C_{ox} - Q_{dep}/C_{ox} + 2\phi_F \quad (1)$$

The depletion charge ( $Q_{dep}$ ) is much smaller than the total oxide charge ( $Q_{tot}$ ) of dielectric on pentacene that contains high-density interface charge ( $Q_{it}$ ), fixed oxide charge and oxide-trapped charge. Since the low temperature deposited dielectric has inevitable poor quality of both bulk oxide and oxide/pentacene interface, the  $Q_{tot}$  is much larger than the  $SiO_2$  on Si to lead the unwanted high  $V_T$ . To achieve the needed low  $V_T$ , here we have largely increased the oxide capacitance ( $C_{ox} = \epsilon_0 \kappa / t_{ox}$ ) by using higher  $\kappa$  HfLaO [6] dielectric with thin thickness ( $t_{ox}$ ). The high  $C_{ox}$  can also improve the SS by:

$$SS = kT/q \times \ln 10 \times [1 + (C_{it} + C_{dep})/C_{ox}] \quad (2)$$

The HfLaO/pentacene OTFTs showed a record low SS of only 0.08 V/decade, a low  $V_T$  of -1.3 V, good field-effect mobility ( $\mu_{FE}$ ) of 0.73  $cm^2/Vs$  and a large  $I_{on}/I_{off}$  of  $1.2 \times 10^5$ . This was achieved by using high gate capacitance density of 950 nF/cm<sup>2</sup>, where the leakage current was decreased by applying a  $NH_3^+$  plasma treatment on TaN gate electrode.

### 2. Experiments

The devices were fabricated on  $SiO_2/Si$  substrates. The TaN gate electrode of 50 nm was first deposited through a shadow mask by reactive sputtering. The TaN surface was treated by  $NH_3^+$  plasma to reduce the dielectric leakage current [7]. Then 20-nm HfLaO was deposition by PVD and  $O_2$  PDA at 350 °C for 10 min. After that, 70 nm thick pentacene active layer was deposited at 70°C with small 0.5 Å/s rate under  $3 \times 10^{-6}$  torr. Finally, Au source-drain electrodes were deposited by thermal evaporation and patterned by shadow mask. Besides, metal-insulator-metal (MIM) Au/HfLaO/TaN capacitor was also fabricated to analyze the leakage current and the dielectric properties.

### 3. Results and Discussion

Fig. 1 shows the schematic diagram of the HfLaO/pentacene OTFTs and MIM devices. Fig. 2 shows the  $J$ - $V$  characteristics of Au/HfLaO/TaN capacitors. The  $NH_3^+$  treatment improves the leakage current of both electron injection from top Au/HfLaO and bottom HfLaO/TaN with close capacitance density shown in Fig. 3. It is important to notice that the leakage current is much worse as electron injected from bottom interface, which is consistent with previous Analog/RF and DRAM MIM capacitors [7]. However, such bottom electron injection is needed for the negative  $V_G$  used in p-MOSFET. Figs. 4, 5 and 6 compare the  $I_D$ - $V_D$  and  $I_D$ - $V_G$  characteristics of HfLaO/pentacene p-MOSFETs with and without  $NH_3^+$  treatment on TaN gate. The device with  $NH_3^+$  treatment improves  $I_D$  on-current ( $I_{on}$ ), SS and off-current ( $I_{off}$ ) simultaneously. Record small SS of only 0.08 V/decade is measured, and the small  $V_T$  of -1.3 V allows the device to operate at -2 V. Note that the  $I_{on}$  improvement is not due to the pentacene, since the surface roughness and grain sizes shown in Fig. 7 is similar without and with  $NH_3^+$  treatment. Table 1 summarizes the comparison of p-channel HfLaO/Pentacene OTFTs with n-channel poly-Si TFTs. The performance of this  $NH_3^+$ -treated p-channel HfLaO/pentacene OTFTs is comparable with that of n-channel  $SiO_2$ /poly-Si TFTs using LPCVD and PECVD TEOS oxides [3]-[5]. The excellent device integrity of record low SS of 0.08 V/decade and low  $V_T$  of -1.3 V are simply due to the very high  $C_{ox}$  of 950 nF/cm<sup>2</sup> in HfLaO dielectric that lowers  $(C_{it} + C_{dep})/C_{ox}$  and  $Q_{tot}/C_{ox}$  terms in eq. (2) and (1), respectively. The TaN treatment on TaN surface is vital to decrease the leakage current at such high  $C_{ox}$  density, which is the basic challenge for MIM capacitors [7]. The much lower thermal budget for OTFT fabrication than Si-TFT is highly favorable for environment energy conservation.

### 4. Conclusions

Low  $V_T$ , low operation voltage, small SS and good mobility are achieved in HfLaO/pentacene OTFTs with  $NH_3^+$  treatment on TaN gate electrode.

### References

- [1] H. Klauk, D. J. Gundlach, J. A. Nichols, and T. N. Jackson, IEEE Trans. Electron Devices **46** (1999) 1258.
- [2] M. Mizukami *et al*, IEEE Electron Devices Lett. **27** (2006) 249.
- [3] Y. W. Choi *et al*, IEEE Electron Devices Lett. **27** (1999) 2.
- [4] C. W. Lin *et al*, IEDM Tech. Dig. (1999) 305.
- [5] K. M. Chang *et al*, IEEE Electron Devices Lett. **27** (2003) 512.
- [6] C. F. Cheng *et al*, IEDM Tech. Dig. (2007) 617.
- [7] K. C. Chiang *et al*, VLSI Symp. Tech. Dig. (2006) 126.

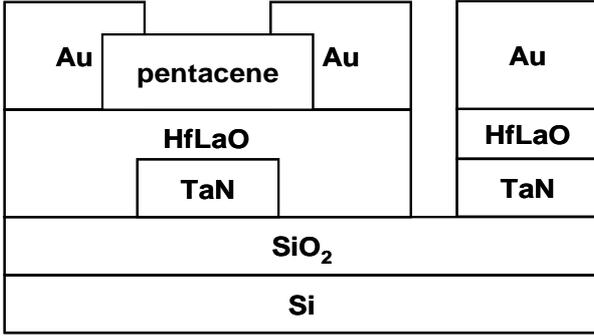


Fig. 1 Schematic diagram of HfLaO/pentacene OTFTs and Au/HfLaO/TaN MIM devices.

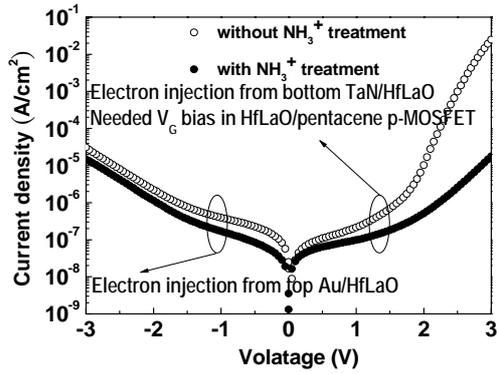


Fig. 2 Leakage current comparison of Au/HfLaO/TaN capacitors with and without  $\text{NH}_3^+$  treatment.

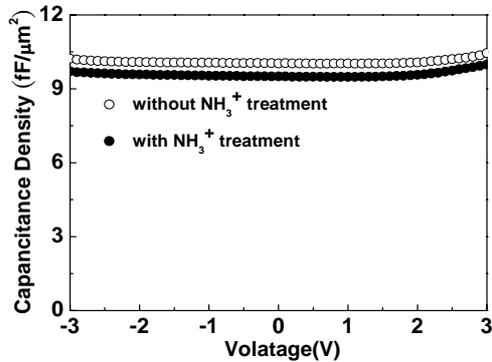


Fig. 3  $C$ - $V$  characteristics of Au/HfLaO/TaN capacitors with and without  $\text{NH}_3^+$  treatment.

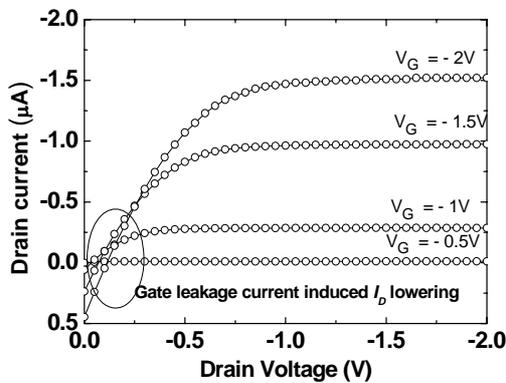


Fig. 4  $I_D$ - $V_D$  characteristics of HfLaO gate dielectric OTFTs without  $\text{NH}_3^+$  treatment.

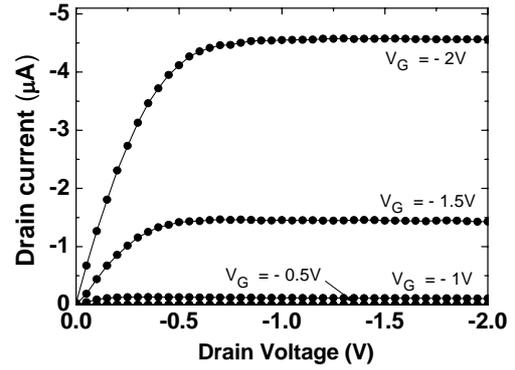


Fig. 5  $I_D$ - $V_D$  characteristics of HfLaO gate dielectric OTFTs with  $\text{NH}_3^+$  treatment.

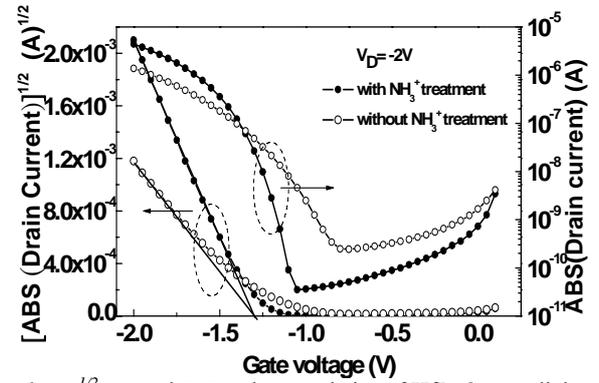


Fig. 6  $I_D^{1/2}$ - $V_G$  and  $I_D$ - $V_G$  characteristics of HfLaO gate dielectric OTFTs with and without  $\text{NH}_3^+$  treatment.

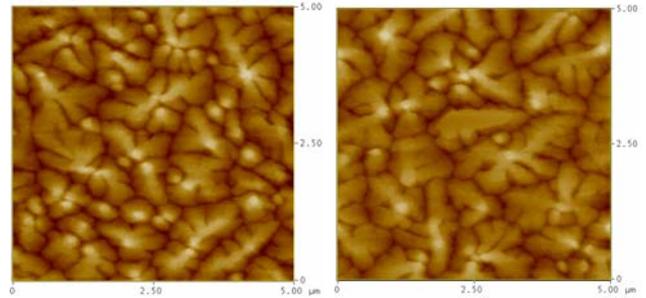


Fig. 7 AFM surface images of pentacene ( $5\mu\text{m} \times 5\mu\text{m}$ ) on HfLaO/TaN with (left) and without (right)  $\text{NH}_3^+$  treatment.

TABLE I Comparison of p-channel HfLaO/pentacene OTFTs with n-channel poly-Si TFTs.

Gate dielectric	HfLaO 20 nm	LPCVD SiO <sub>2</sub> 80 nm [3]	PECVD TEOS oxide 60 nm [4]	PECVD TEOS oxide 40 nm [5]
$C_i$ (nF/cm <sup>2</sup> )	950	43.1	57.5	86.3
$V_T$ (V)	1.3	5.6	8.14	-
$\mu_{FE}$ (cm <sup>2</sup> /Vs)	0.73	20	12.44	3
SS (V/decade)	0.08	1.4	1.97	2.67
$\mu_{FE}C_i$ (nF/cm <sup>2</sup> )	693.5	862.8	715.7	258.8
$I_{on}/I_{off}$	$1.2 \times 10^5$	$3.5 \times 10^5$	$2.97 \times 10^5$	-