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Suppression of the performance dispersion of organic field-effect transistors employing annealing process

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1. Introduction

Organic FETs have been paid much attention as one of key technologies for realizing flexible, printable and large-area electronics. To realize such applications, stability and reliability of the organic FETs are very important. Because of many degradation factors, such as oxygen- or moisture- associated species and DC bias stress effects, so transistor characteristics of organic FETs have large dispersion even if they are fabricated with identical structural parameters and processes. In the previous work, we have improved the characteristics of one transistor and suppressed the DC bias stress-induced degradation in pentacene FETs using annealing process[1,2].

In this work, we demonstrated the suppression of the performance dispersion of pentacene FETs employing annealing process.

2. Fabrication process

Pentacene FETs were fabricated by vacuum evaporation process. First, a 5-nm-thick Cr and a 50-nm-thick Au were deposited as a bottom-gate electrode through a shadow mask in a vacuum evaporator on a 75-μm-thick polyimide film. Then, polyimide precursors were spin-coated to form 500-nm-thick polyimide layers as the bottom gate insulators. Purified pentacene was deposited to form 50-nm-thick channel layers and a 50-nm-thick Au layer was evaporated to form source-drain electrodes. Finally, FETs were annealed at 140 ºC for 3.5 hours in nitrogen environment. The Cannel widths were 500 nm for all FETs, and the Channel lengths (L) were from 10.5 μm to 120 μm. Fig. 1 shows the cross-sectional view of the device structure and the optical microscope image of the device with channel length of 10.5 μm.

3. Results

The transistor properties and DC bias stress degradation properties of the pentacene FETs were measured using a precision semiconductor-parameter analyzer (Agilent Technologies, 4155c). All measurements were carried out in nitrogen environment, so oxygen- or moisture-associated species which cause transistor degradation were less than 1 ppm.

Fig. 2 shows the typical characteristics of transistors after annealing. The source-drain current (I_{DS}) was measured as a function of the source-drain voltage (V_{DS}), as shown in Fig 2 (a). The gate voltage (V_{GS}) is varied from 0 to −40 V in steps of −10 V. Fig. 4 (b) shows the transfer curves of the FETs with channel length (L) = 10, 20, 32, 45 and 120 μm, respectively. V_{GS} was varied from 20 to −40 V with the application of V_{DS} = −40. The on-off ratio exceeds 10^6.

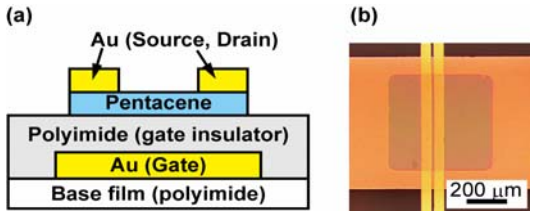

fig.1. (a)The cross-sectional illustration of the organic transistor. (b)The optical microscope image of organic FET with channel length of 10.5 μm.

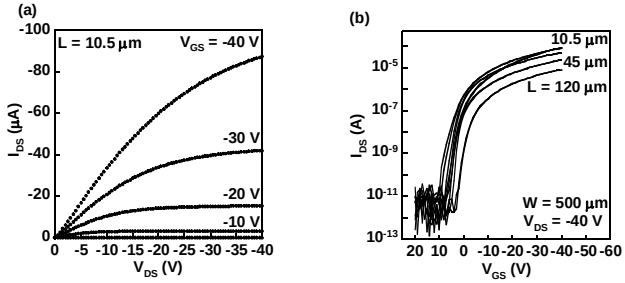

Fig.2. characteristics of the pentacene FETs after annealing.

Fig. 3 shows the dispersion of mobilities of pentacene FETs before and after annealing in the saturation regime. The mobility before annealing was dispersed in wide range from 0.3 to 1.4 cm^2/Vs, especially with small channel length (fig 3 a). However, after annealing, the variation in mobility is significantly suppressed to between 0.4 and 0.5 cm^2/Vs (fig.3 b).

Fig. 4 shows the resistance evaluated from saturation regime. The contact resistance was improved using annealing effect, and the value was identical to the minimum values (contact resistance of pentacene FETs with evaporated Au top contacts) reported by other groups [3-5], which indicates the high quality of the interfaces between the Pentacene and Au electrodes.

Fig. 5 shows the change in I_{DS} of the FETs with channel length of 32 μm before and after annealing under continuous DC voltage biases of V_{GS}=V_{DS}=−40 V. the DC bias degradation was suppressed using annealing effect.

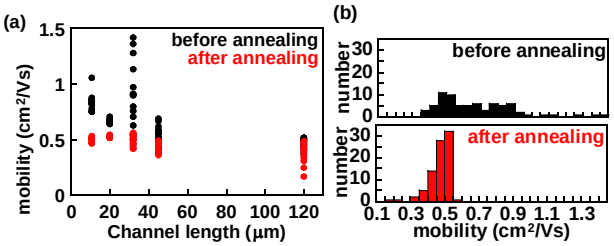

Fig.3. The mobility of pentacene FETs before and after annealing. (a) the mobility in saturation region as the function of channel length (L). (b) The histogram of mobilitiy before and after annealing.

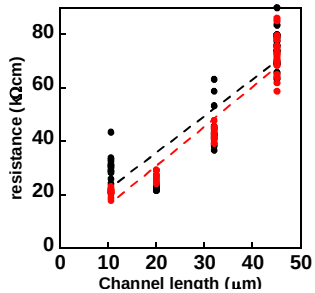

Fig. 4. The resistance in the saturation regime scales linearly with channel length. The dot lines are line fitting of before and after annealing.

5. Discussion

In the case of organic FETs, many degradation processes are induced by oxygen and moisture-associated atmospheric species [6]. Furthermore, electrical instability of the transistor is also induced by the application of a DC bias stress [7,8]. Although the stability of organic transistors can be controlled by passivation layers [9], the gas permeability of passivation layers is not sufficiently low. Furthermore, such instabilities in air may cause large variation in transistor characteristics on organic transistors.

As shown in Fig. 3, we clearly demonstrate the suppression of the variation in the performance employing annealing process, which may be due to the elimination of the atmospheric components through the high temperature annealing. In fact, annealing process led to the decrease in parasitic contact resistance (Fig. 4) although contact resistance at the interface between organic semiconductors and metal is significantly affected by air-degradation.

Although DC bias stress effect (changes in V_{th} and I_{DS} under continuous voltage application) have not yet been achieved in organic transistors thus far [7,8], we have clearly observed to suppress the DC bias stress effect on organic FETs, which may be due to the elimination of deep-trapping potential sites associated with atmospheric components. In fact, in amorphous- and polycrystalline-silicon-based transistors, the changes in V_{th} and I_{DS} associated with DC bias stress can be understood well by the qualitative analysis of the deep trapping of conduction carriers [10], where major progress has been made to

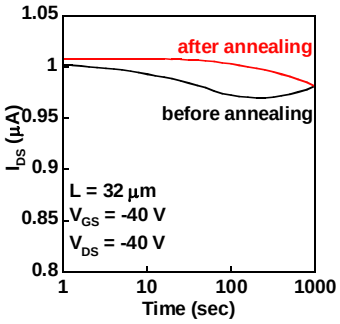

fig.5. Change in source-drain current (I_{DS}) after continuous DC biases (V_{GS}=V_{DS}= −40 V) as function of time t. I_{DS0} represents I_{DS} at the start of the measurement (t = 0).

suppress the degradations by the surface modification of gate dielectric layers and device annealing for eliminating vacancies and/or lattice defects as candidate deep-trapping potential sites.

6. Conclusion

Employing annealing process, we have successfully improved the electrical characteristics and reliabilities of pentacene field-effect transistors (FETs) on plastic films; the variation in transistor characteristics is suppressed. Furthermore, the DC bias stress effect and parasitic contact resistance are significantly decreased through the annealing.

Acknowledgement

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