Extended Abstracts of the 2008 International Conference on Solid State Devices and Materials, Tsukuba, 2008, pp. 220-221

I-2-8

A Novel Active Matrix Organic Light Emitting Diode Pixel Structure Employing Top-Anode Contact OLEDs

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1. Introduction

Active matrix organic light emitting diode (AMOLED) displays have been considered as future displays that would someday substitute the current existing displays such as LCD and PDP. Due to its high contrast ratio, wide viewing angle, fast response time and low power consumption many research groups have been working and some are now producing AMOLED displays for consumer use [1-4]. Recently, poly-Si based AMOLEDs were developed presenting high reliability and high current driving capability. However the non-uniformity of poly-Si TFT is known to be a major problem in realizing large area displays since non-uniform TFT characteristics lead to non-uniform displays image. In this paper, amorphous silicon thin-film transistors (a-Si TFTs) are used to drive the AMOLED device, since uniformity issues are more important in realizing large area displays than reliability problems.

In this paper, we report on a new compensation method that suppresses both the Vth shift of a-Si TFT and I x R drop in power line for large area AMOLED displays. It consists of six a-Si TFTs, a storage capacitor and a pulsed Vdd signal. The simulation and experimental results show that the pixel design successfully compensates for OLED current variations caused by Vth shift of a-Si TFT and I x R drop in power line.

2. Pixel Structure and Operation

Fig. 1 shows the proposed AMOLED pixel structure and timing diagram. The proposed pixel consists of six a-Si TFTs, one capacitor and one inverted OLED. T1 and T3~6 are switching TFTs and T2 is a driving TFT. Since the OLED is connected to the drain electrode of Driving TFT T2, it is possible to deliver a constant current despite OLED degradation. The operation scheme and compensation principle are described as follows.

Initialization period

During the first period, resetting action is performed in order to refresh the data stored in gate electrode (Vp) of Driving TFT T2. When Vref is set to 0 V, charge stored in storage capacitor Cstg can be estimated to be as follows:

$$V_{Cstg} \approx Vdd - V_{OLED} - V_{on\_T4} \qquad (1)$$

where, VOLED represents the OLED turn-on voltage, and Von_T4 represents the turn-on voltage of diode-connected TFT T4.

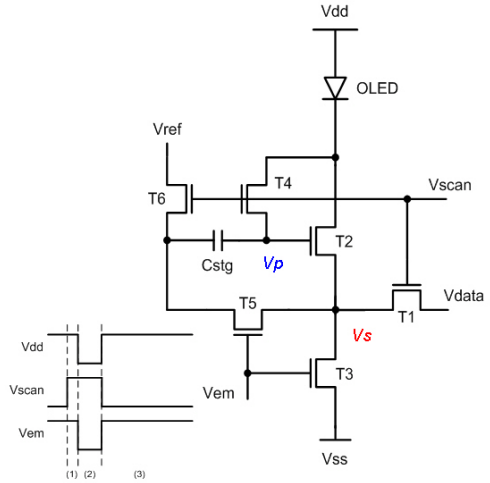

Fig. 1 Proposed AMOLED pixel structure and timing diagram.

Data sampling period

When Vdd and em are set low and scan set high, T3 and T5 are turned off, thus Vdata is sampled by diode-connected TFT T2. At this time, the gate voltage of Driving TFT T2 is programmed to Vdata + Vth_T2 and stored by capacitor Cstg.

Emission period

After data sampling, scan signal is set low and Vdd, em are set high for OLED emission. During this period, Driving TFT T2 starts to drive the OLED and the drain current of Driving TFT T2 in the saturation region becomes as follows:

$$I_{OLED} = \frac{1}{2}k_2\left(V_{GS\_T2} - V_{TH\_T2}\right)^2$$
$$= \frac{1}{2}k_2\left(V_{data} + V_{TH\_T2} - V_{TH\_T2}\right)^2 = \frac{1}{2}k_2 {V_{data}}^2 \qquad (2)$$

The drain current of T2 is independent of the threshold voltage of T2

Also, the I x R voltage-drop in the power line is one of the important issues in realizing large area AMOLED displays. Since large area displays have relatively large I x R voltage drop, this causes voltage rise in the Vss line resulting in OLED current variation. However, in the proposed pixel structure since the data is induced to the source of Driving TFT T2, the influence of Vss voltage drop can be neglected.

Table I Parameters for Spice Simulation

Device size					
W/L (T1)	W/L (T2)	W/L (T3)	W/L (T4)	W/L (T5)	W/L (T6)
30 / 5 um	180 / 5 um	120 / 5 um	15 / 5 um	15 / 5 um	20 / 5 um
Control signal line					
Vdd	Vss	Vscan	Vemi	T_{scan}	T_{em}
0 ~ 20 V	0 V	-5 ~ 15 V	-5 ~ 15 V	70 usec	160 usec

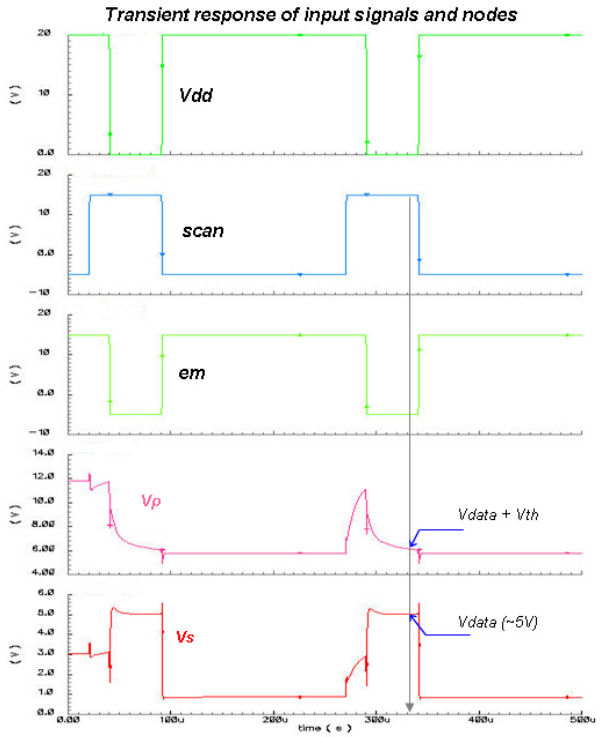

Fig. 2 Transient response of Vp and Vs during data sampling period

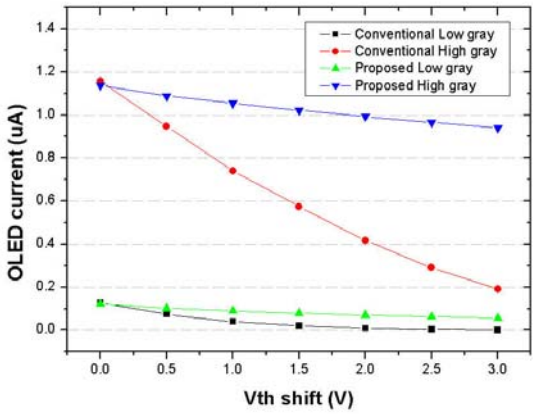

Fig. 3 OLED current variation when Vss rises at high gray and low gray levels.

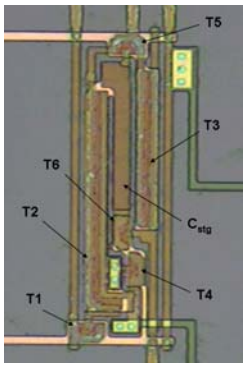

Fig. 4 OM image of the fabricated pixel structure. The pixel size is 85 um x 254 um and OLED is deposited on top.

3. Circuit Simulation and Fabrication Results

After pixel design, SPICE simulation by Cadence® Spectre® was conducted to verify the pixel circuit. The simulation model parameters were extracted from fabricated OLEDs and a-Si:H TFTs. The mobility and threshold voltage of a-Si:H TFT were 1.27 cm2/V·s and 1.01 V, respectively for W/L = 30 / 6 TFTs. Table I lists the parameters used for spice simulation. Fig. 2 shows the transient response of gate node (Vp) and source node (Vs) of Driving TFT T2 during data sampling period. Fig. 3 shows the OLED current variation when Vss rises at high gray and low gray levels. The I x R drop was modeled by Vss rise in power line and 1 V of Vss rise was appropriate for large area displays. The OLED current variation of the proposed pixel due to Vss rise is under 10 % while over 35 % is observed for conventional 2T1C pixel. Fig. 4 shows an OM image of the fabricated pixel structure. The pixel size is 85 um x 254 um and OLED is deposited on top for top-anode contact.

4. Conclusions

New AMOLED pixel structure employing amorphous silicon thin-film transistors (a-Si TFTs) is proposed and verified by SPICE simulations. The proposed circuit shows high immunity to the threshold voltage shift of a-Si TFT and I x R voltage-drop in power lines which will lead to uniform display image. For large area AMOLED displays, the I x R voltage-drop problem in power lines along with threshold voltage degradation will become more severe. Therefore, I x R voltage compensation at the pixel level, such as that in our proposed pixel structure would be more important in realizing large area displays.

Acknowledgements

The authors would like to thank the R&D Center of LG.Philips LCD for their technical support.

References

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