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Design of Insulator Surface for Stable Operation of Organic Field Effect Transistors

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1. Introduction

Organic field-effect transistors (OFETs) have attracted considerable attention due to their application as driving devices in displays, radio-frequency identification tags, and large-area sensors. Recently, the mobility of OFETs has become comparable to that of amorphous Si transistors. However, their stability remains poor. We previously reported that there are two components of electrical instabilities for OFETs [1]. One is instability caused by mobile dipole of insulator surface. When the insulator surface has mobile dipoles, decrease in source-drain current (I_{SD}) of OFET with respect to time was caused by application of bias voltage [1]. The other is threshold voltage shift caused by gate bias stress. The application of a negative gate bias causes a negative shift in the threshold voltage (V_t) and a decrease in the I_{SD} [2]. These two instabilities have different time scale for decrease in I_{SD}. The decrease in I_{SD} due to surface dipole of insulator occur fast time scale (less than approximately 1 s after the application of bias voltage). On the other hand, V_t shift caused by gate bias stress is very slow time scale change; the change of V_t continues over several hours. In order to obtain stable operation of OFETs, it is necessary to suppress both instabilities.

Since the conducting channel formed in the organic layers lies very close to the semiconductor / insulator interface, the characteristics of an OFET are strongly influenced by the surface of the insulator. Thus, we tried to suppress the fast and the slow instabilities by controlling of insulator surface. We previously reported that, the fast time scale instability can be suppressed by removing of dipole from insulator surface [1]. Following this, we investigated the influence of insulator surface on V_t shift caused by gate bias stress (slow time scale instability).

In this presentation, we report effect of roughness and chemical species of insulator surface on V_t shift caused by gate bias stress. We will also report the effective method for suppression of the fast and slow instabilities by modification of insulator surface.

2. Experimental

Top contact transistors with a pentacene semi-conducting layer were fabricated on a highly n-doped Si substrate with a 200 nm-thick SiO_2 layer. In order to investigate the influence of surface roughness of insulator on V_t shift, fine roughness was introduced in the SiO_2 surfaces by wet-etching using an etching solution comprising H_2O_2, NH_4OH, and H_2O. In order to investigate the influence of chemical species of insulator surface on V_t shift, various types of self-assembled monolayers were introduced to the SiO_2 surface.

3. Influence of surface roughness of insulator on V_t shift caused by gate bias stress

Figure 1 shows AFM images of SiO_2 surfaces with RMS roughness values of 0.16 (Which is most flat SiO_2 used in this study) and 0.22 nm (which is most rough SiO_2 used in this study). From the height profiles of both images, the difference in roughness between the two images was of the order of sub-nanometers.

We measured influence of SiO_2 roughness on V_t shift caused by gate bias stress of -30 V for 20 min. The V_t shift was increased by increase in roughness of SiO_2. For a device with an RMS roughness value of 0.16 nm, the V_t shift was only −3.5 V; however, it increased to −10.3 V for devices with an RMS roughness value of 0.22 nm. Therefore, it can be concluded that the V_t shift, which is caused by gate bias stressing, is very sensitive to the fine roughness of the insulator surface and increases with the roughness.

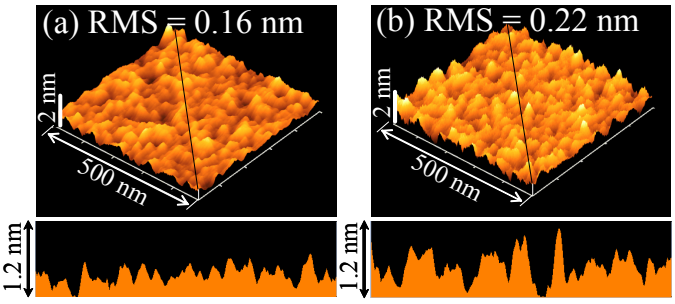

Figure 1 AFM images of SiO_2 surfaces. The height profiles at the lines in these images are shown under each image.

By measurement of X-ray diffraction and atomic force microscopy, we observed that the surface rough-

roughness of SiO_2 caused two morphological changes in the pentacene layer—a decrease in the grain size of pentacene and an increase in the lattice distortion in the pentacene layer. We measured the V_t shift for OFETs with pentacene of different grain sizes and identically rough SiO_2 substrates (RMS = 0.16 nm). As a result, the V_t shift is not significantly influenced by the grain size of pentacene. We will discuss about the relationship between lattice distortion of pentacene and V_t shift caused by gate bias stress.

4. Influence of surface chemical species of insulator on V_t shift caused by gate bias stress

Figure 2 shows the relationship between the chemical species of the insulator surface and the amount of V_t shift after applying a gate voltage (V_G) of −20 V and source-drain voltage (V_D) of 0 V for 15 min [2]. The most interesting feature in Fig. 2 is the dependence of the V_t shift on the SAM chain length. The V_t shift increased with the length of the SAM molecules. For HMDS devices (which have the shortest SAM molecules), the V_t shift was only −2.1 V; however, it increased to −5.4 V for OTS devices (which have the longest SAM molecules). This indicates that the stability of OFETs deteriorated because of the long-chain chemical species of the insulator surface. However, when focusing on SAMs with similar chain lengths (Allyl–SAM, Propyl–SAM, and Chloro–SAM), a significant difference was not observed in the amount of V_t shift, even if the terminal of the SAMs was different.

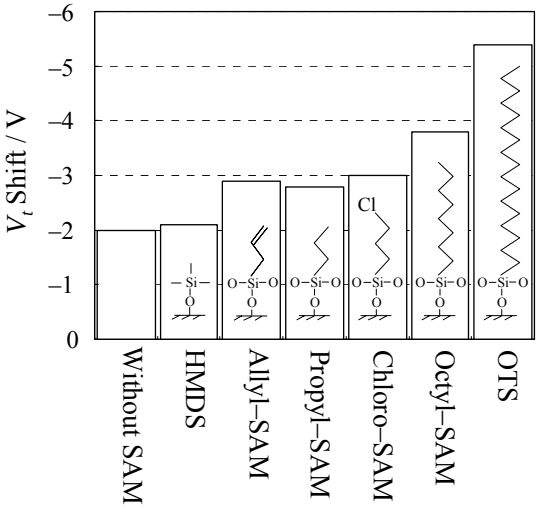

Figure 2 Relationship between the chemical species of the insulator surface and the *Vt* shift. The amount of *Vt* shift was measured after stressing at V_G = −20 V and V_D = 0 V for 15 min.

5. Suppression of V_t shift by polystyrene coating of SiO_2 surface

We previously reported that dipole of insulator surface cause the fast time scale instability [1]. From this result associated with fast time scale instability and present results associated with slow time scale instability (V_t shift caused by gate bias stress), we concluded that the insulator surfaces should posses the following three characteristics for realization of stable operation. First, they should not have dipoles at insulator surface. Second, the surfaces should be flat. Third, they should not have long-length chemical species. One candidate of insulator material which satisfies above condition is polystyrene (Fig. 3) having flat surface. Polystyrene do not have strong dipoles and long substituted groups in the side chain. We observed that polystyrene fabricated by spin coating on an SiO_2 substrate have flat surface as compared to a bare SiO_2 surface.

Figure 3 shows V_t shift as a function of time for OFETs with and without coating of SiO_2 surface with a 20 nm-thick polystyrene layer. The amount of V_t shift for polystyrene coated OFETs was approximately 20 % as compared to that for OFETs without coating. Moreover, mobility was enhanced from 0.2 to 1.3 $cm^2V^{-1}s^{-1}$ by polystyrene coating.

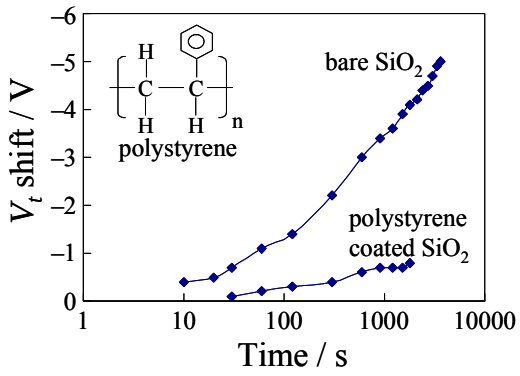

Figure 3 Threshold voltage shift as a function of time. The stress bias were V_G = −20 V and V_D = 0 V.

6. Conclusion

We investigated influence of insulator surface on the stability of OFETs. The roughness and long chemical species of insulator surface deteriorate the stability of OFETs. The OFETs with a polystyrene insulator having flat surface showed high stability and high performance.

References

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