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Overview and Future Challenges of DRAM Technologies

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1. Abstract

This paper reviews key technologies for future DRAM. To continue to be the dominant memory, competitive advantages such as performance and power consumption of DRAM over other co-existing memories will be reassessed in the viewpoint of cost effectiveness. Then, the technical challenges to encounter on the way to scaling down DRAM will be mainly discussed with expectation to overcome those by developing new material, processes, device structures and design. Through these we reach to the conclusion that DRAM will still have the strong merits in performance and power consumption comparing with various other memories including new memories at least down to 30nm node and beyond.

2. Introduction

As well known, a memory is used as a storage element of information. With ever-increasing amount of the newly generated information across the world, the demands for high density and high performance memory are exploding rapidly. Since the birth of computer, it has been pursued to have ideal Si memory whose characteristics will be small die size, small cell size, low latency, high data-rate, low operating power, low standby power, non-volatility, unlimited usage and so on. Unfortunately, up to now there is yet ideal memory which satisfies all of these at the same time. Among commercially available random access memories (SRAM, DRAM, NOR), SRAM has highest bandwidth and NOR flash memory has lowest operating power per bandwidth as shown in figure 1(a). However, considering the cost, DRAM has highest bandwidth and lowest operating power as shown in figure 1(b). This is the reason why DRAM has been the leading memory device since 1970s. Therefore, the most important thing for future DRAM is cost effectiveness or scalability to have the continued competitive power in the future. This paper compares the bandwidth and power consumption of DRAM with other memories, and predicts the positioning of DRAM in future.

3. Scalability (Technology) [1~3]

The first concern in the prospect of future DRAM is how far we can extend the DRAM technology in future. Key features of DRAM cell scaling are to increase the capacitance of storage capacitor and to reduce the leakage current at the storage node.

In order to achieve the sufficient storage capacitance (>25fF/cell), it is needed to develop the innovative capacitor structure and dielectric material. With a novel capacitor structure such as mesh type cell capacitor and the recent advances of DRAM cell capacitor technology, it is expected that DRAM cell capacitor technology will be available at least down to 30nm node by using the high-k dielectric material and MIM electrode as shown in figure2.

To achieve the low leakage current, various cell transistor structures and improvement of process have been developed. Figure3 shows the evolution trends of cell transistor structure down to 30nm node. In addition to these cell transistor structures, various process optimizations have also been developed such as elevated source/drain by using SEG and asymmetric source/drain. With innovations on the cell transistor structure, cell capacitor structure, capacitor dielectric and electrode material, DRAM can be extended at least to 30nm node and beyond.

4. Cost Effectiveness

The strongest advantage of DRAM is its low cost per performance. Cost is determined by many factors – the number of net dies per wafer (cell size and cell array efficiency), number of process steps, process complexity, test time and yield. DRAM has low cost due to the small cell size, high cell array efficiency and high yield. Therefore, the second concern is “Can we sustain the advantage of low cost in the future?”. To correctly answer this question, at least we have to consider two big issues: *increased investment cost and challenges from other memories as well as emerging new memories*.

It is worried about that the investment cost has increased steeply since 2000. Especially, it has been expected that the price of photo lithography tool increases sharply from KrF to ArF and ArF to EUV. However, as it has been proven, we have continuously reduced the investment cost per chip hour due to the many combined efforts such as increase of wafer size, improving the throughput, increased productivity on site and etc. As a result, it is very natural that CoO (cost of ownership) of lithography which is primary factor of fabrication cost can follow the traditional decline trend as shown in figure 4.

The second concern is competitors of DRAM. Other memories also exert all their powers to reduce their costs. SRAM uses stacked cell structures to reduce the cell size from 90F2 to 25F2. Flash memory improves the bandwidth by increasing the number of bits for parallel data processing. Emerging new memories threat DRAM in power consumption with the help of non-volatility.

Figure5 compares the expected bandwidth/cost for various memories. Flash memories and PRAM can beat DRAM in read bandwidth/cost. However, it is thought to be difficult for Flash memories and PRAM to replace DRAM due to some constraints. DRAM is mainly used as a buffer memory for computing environments, which is commonly used to store data for quick and temporary access. Requirements for buffer memories are high bandwidth for write and read, fast read latency and good endurance. NAND flash memory has weakness in write bandwidth and read latency, even though NAND flash memory might have higher read bandwidth per cost than that of DRAM. Random access time of NAND flash memory is several tens of micro-second, and write bandwidth of NAND is lower than that of DRAM. Furthermore, NAND flash memory constrains the number of cycles in write process and needs block unit operations in write process and erase operation. This circumstance is the same for PRAM. Write bandwidth and endurance make the usage of PRAM difficult as the buffer memory. As a result, DRAM can still have enough competitive power in buffer memory application in the future.

On the other hand, power consumption will be more and more important in future due to prevailing mobile applications in future. Idle mode or standby mode power consumption is more important than active mode in order to maximize lifetime of battery. DRAM has inherent drawback in standby mode power consumption due to the self refresh. This weakness, however, can be much improved by increasing the retention time and several design techniques as shown in figure 6.

5. Conclusions

Technical challenges and cost effectiveness for future DRAM have been reviewed. Despite of many concerns, innovative breakthrough in material, process, device structure and new design techniques will continue the cost effective performance and power consumption in the future at least down to 30nm node and beyond.

References

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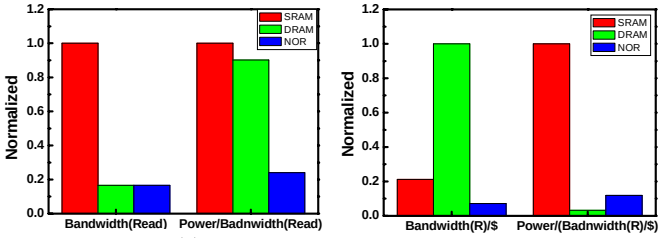
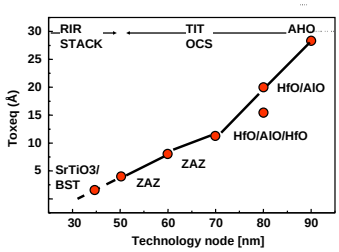
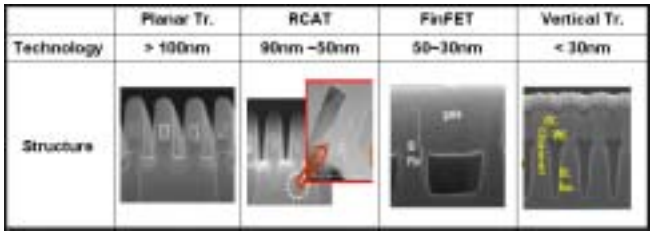


(a) (b)

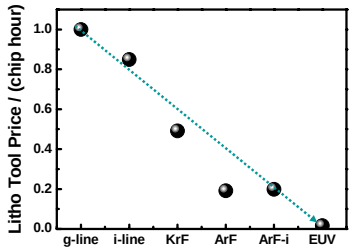
(Fig.1) (a) Comparison of read bandwidth and power consumption per bandwidth, (b) Bandwidth and operating power per cost



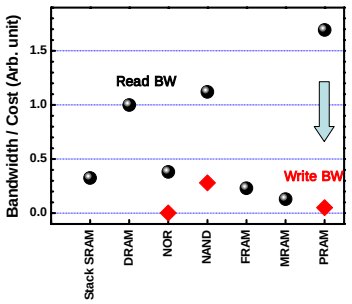
(Fig.2) Direction of cell capacitor evolution: high-k dielectirc



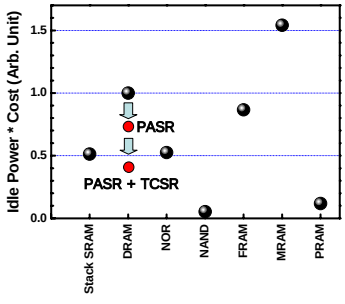
(Fig.3) Evolution of DRAM cell transistor structures



(Fig.4) Trends of Lithography Tool Price per chip hour



(Fig.5) Comparison of Bandwidth / cost for various memories



(Fig.6) Comparison of Idle mode power consumption*cost for various memories